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ABSTRACT:

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(54) **Transceiver element**

(57) A transceiver element for coupling electromagnetic energy between an antenna 26i and a radar system has a phase shifter 40, a transmitter amplifier 24 and a receiver amplifier 28. Four switching devices 18a, 18b, 18c and 18d are controlled by the radar system 11, which supplies control signals 29 thereto, and operate to steer electromagnetic energy from the radar system from an input terminal 33i, through the phase shifter 40 and the transmitter amplifier 24 and to an output terminal 35i to the antenna 26i during a transmit mode, and from the output terminal 35i through the receiver amplifier 28 and the phase shifter 40 to the input terminal 33i during a receive mode, so that the electromagnetic energy passes through the phase shifter 40 in the same direction during the transmit and the receive mode.
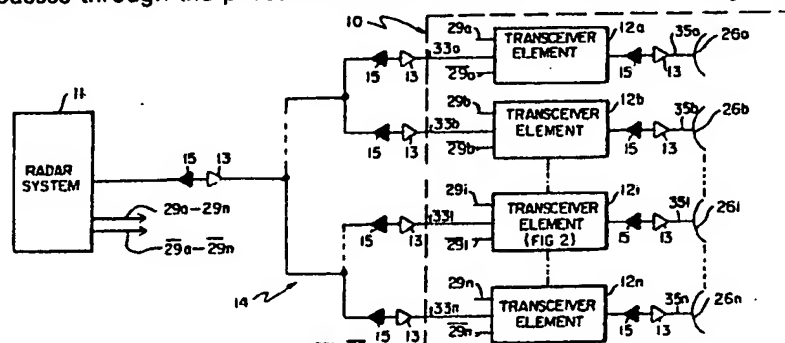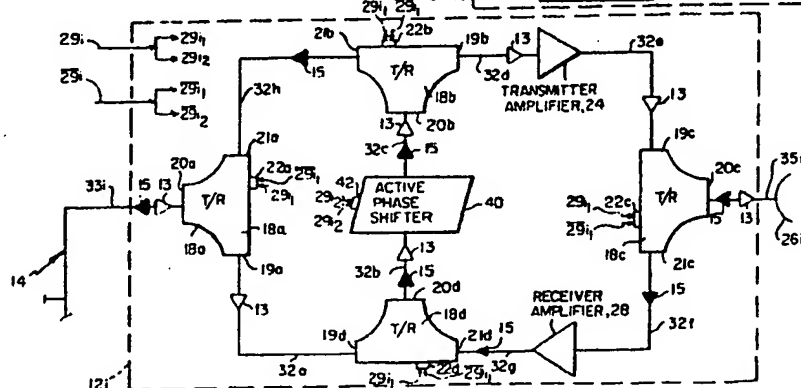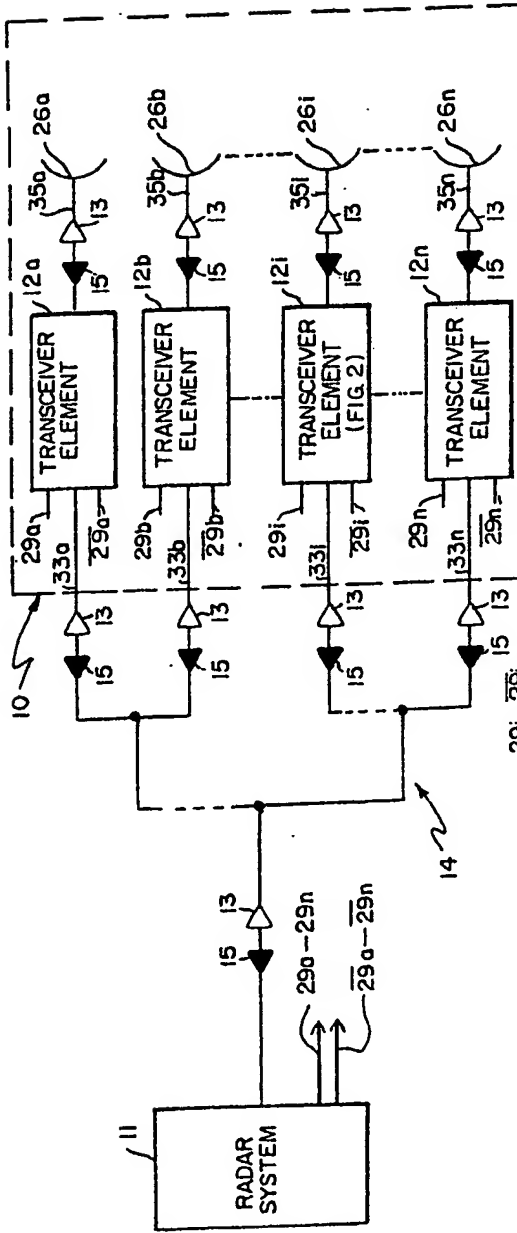
FIG.1

FIG.2

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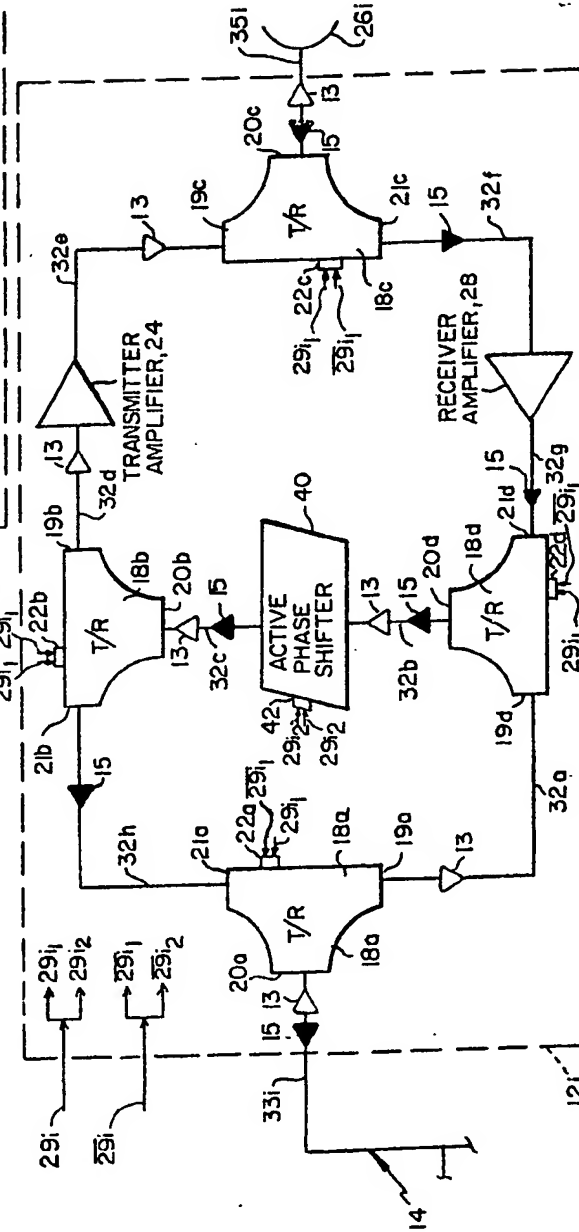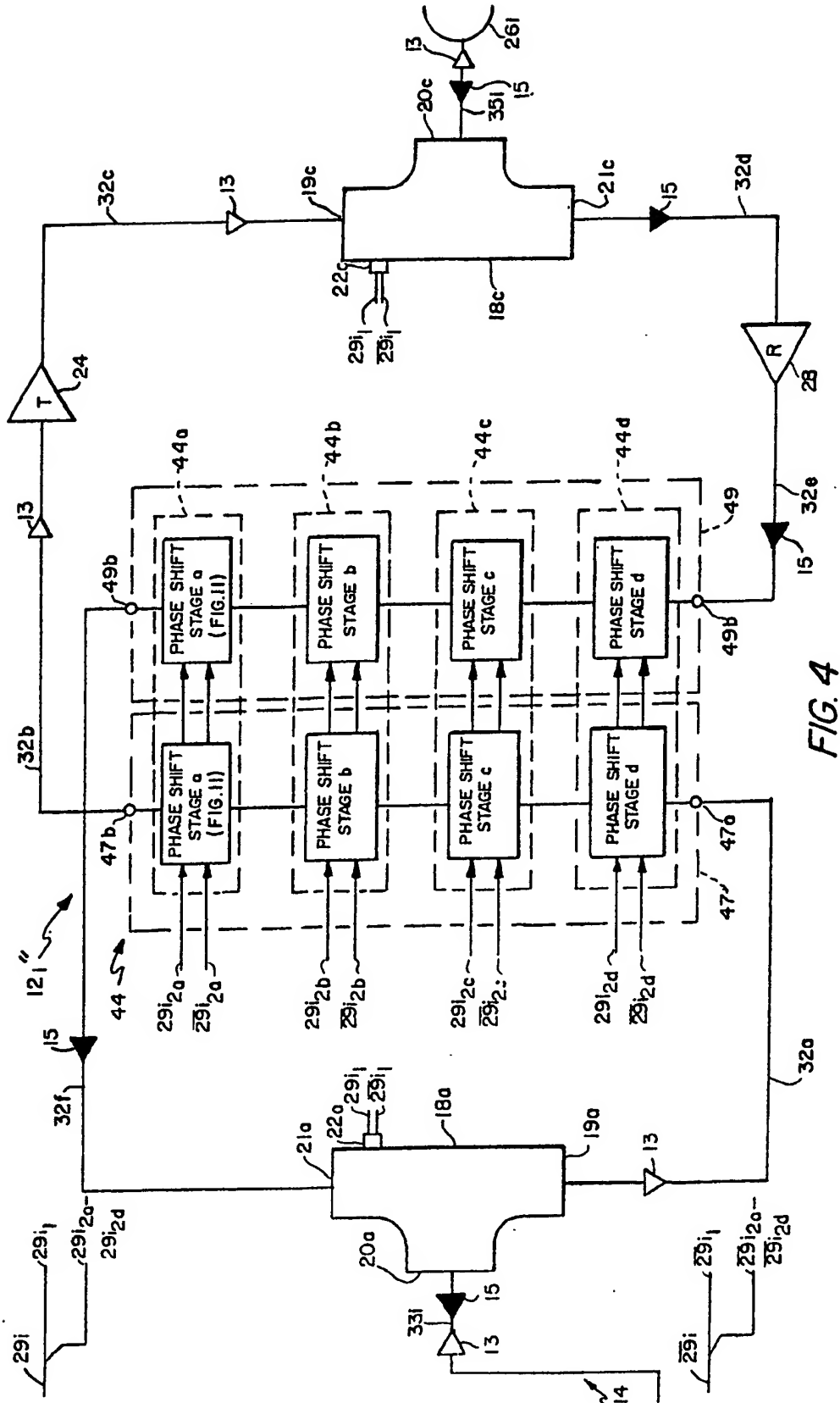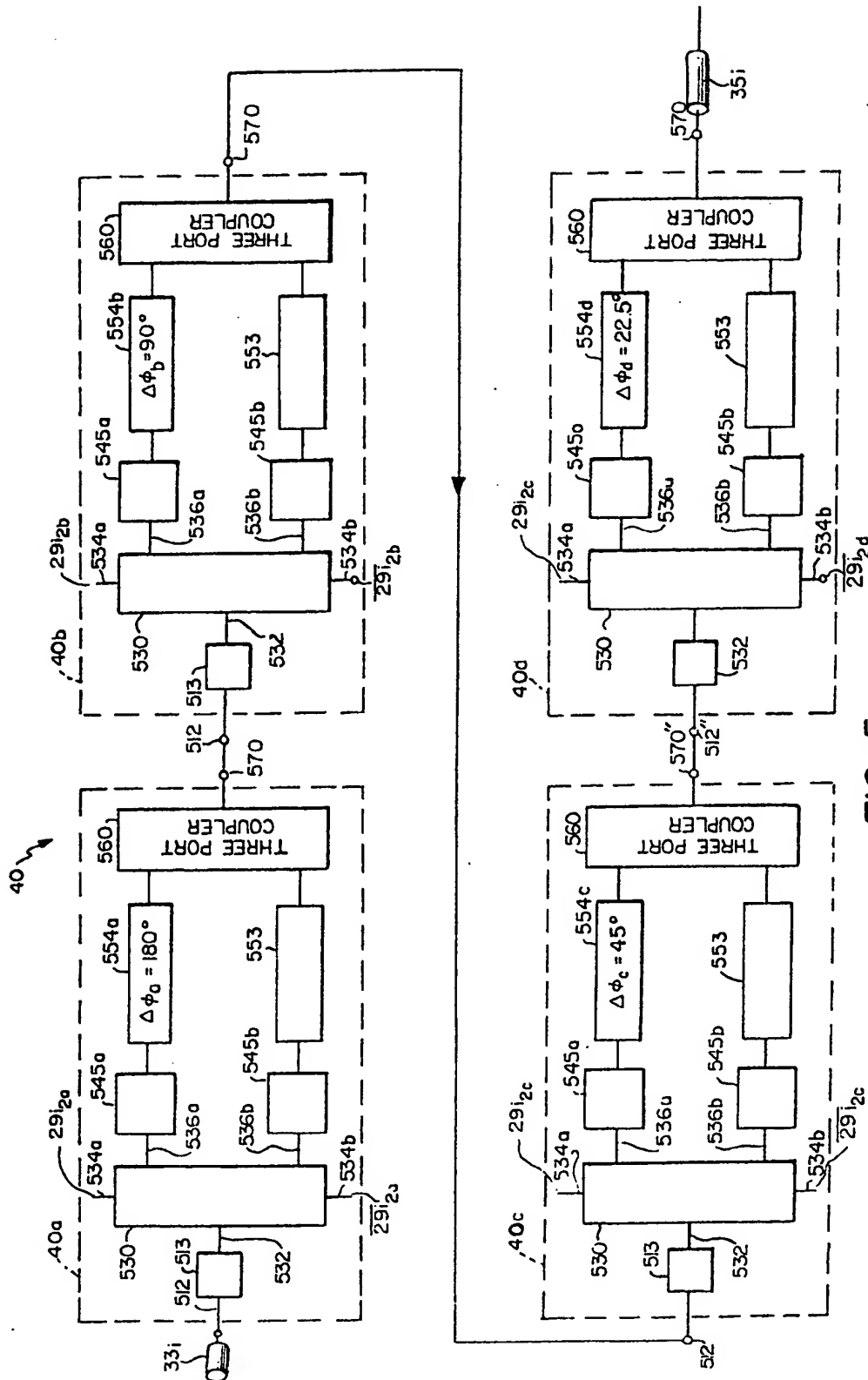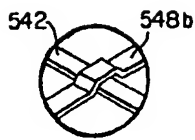*FIG.1*

FIG.2

FIG. 3

FIG. 4

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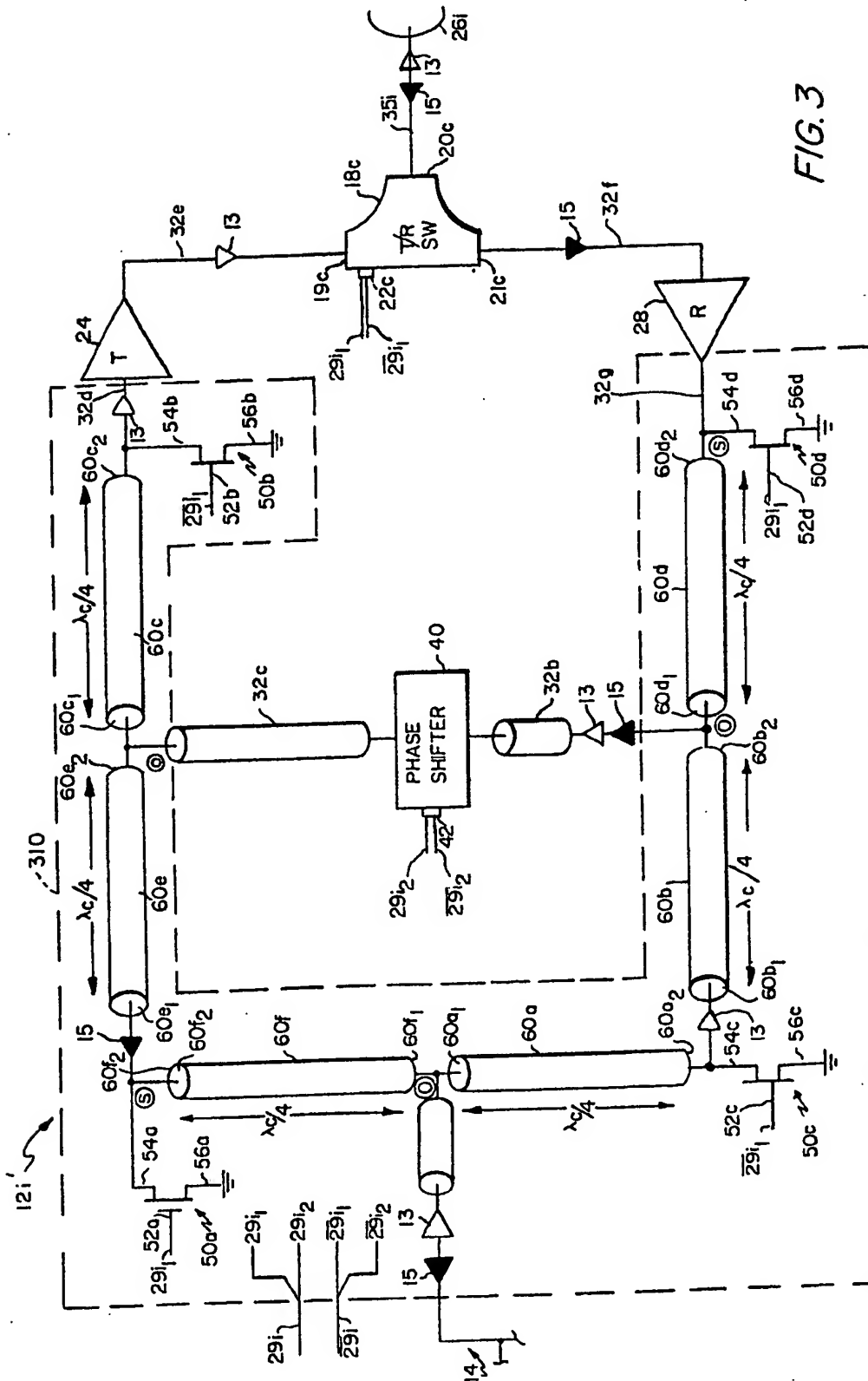
FIG. 5

FIG. 6

FIG. 6A

FIG. 6B

FIG. 7
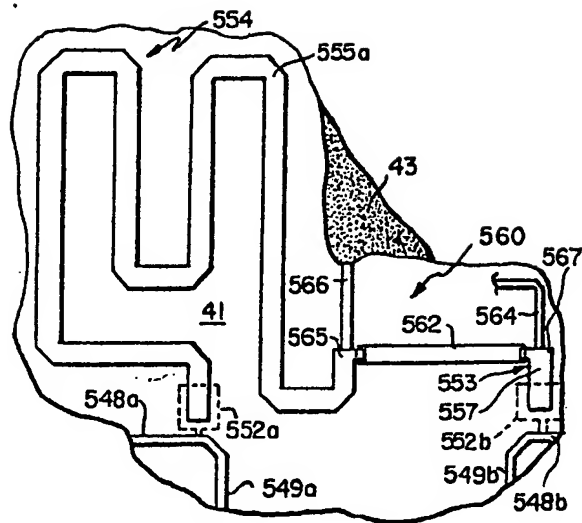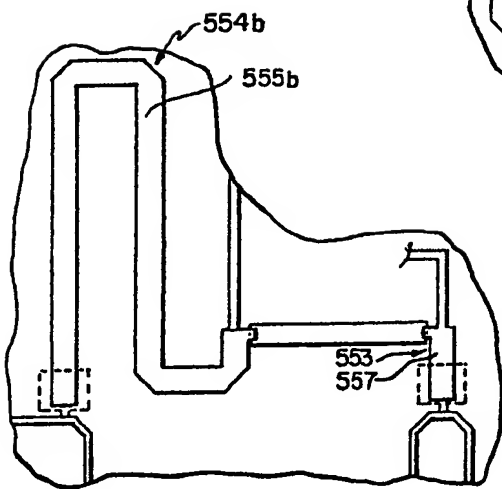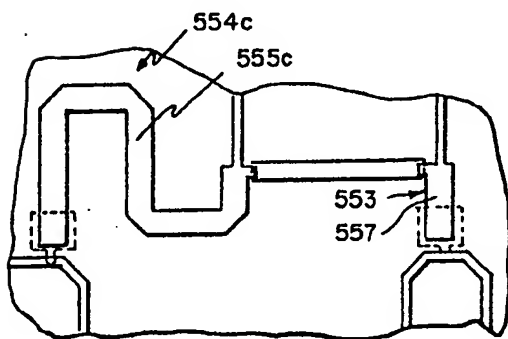
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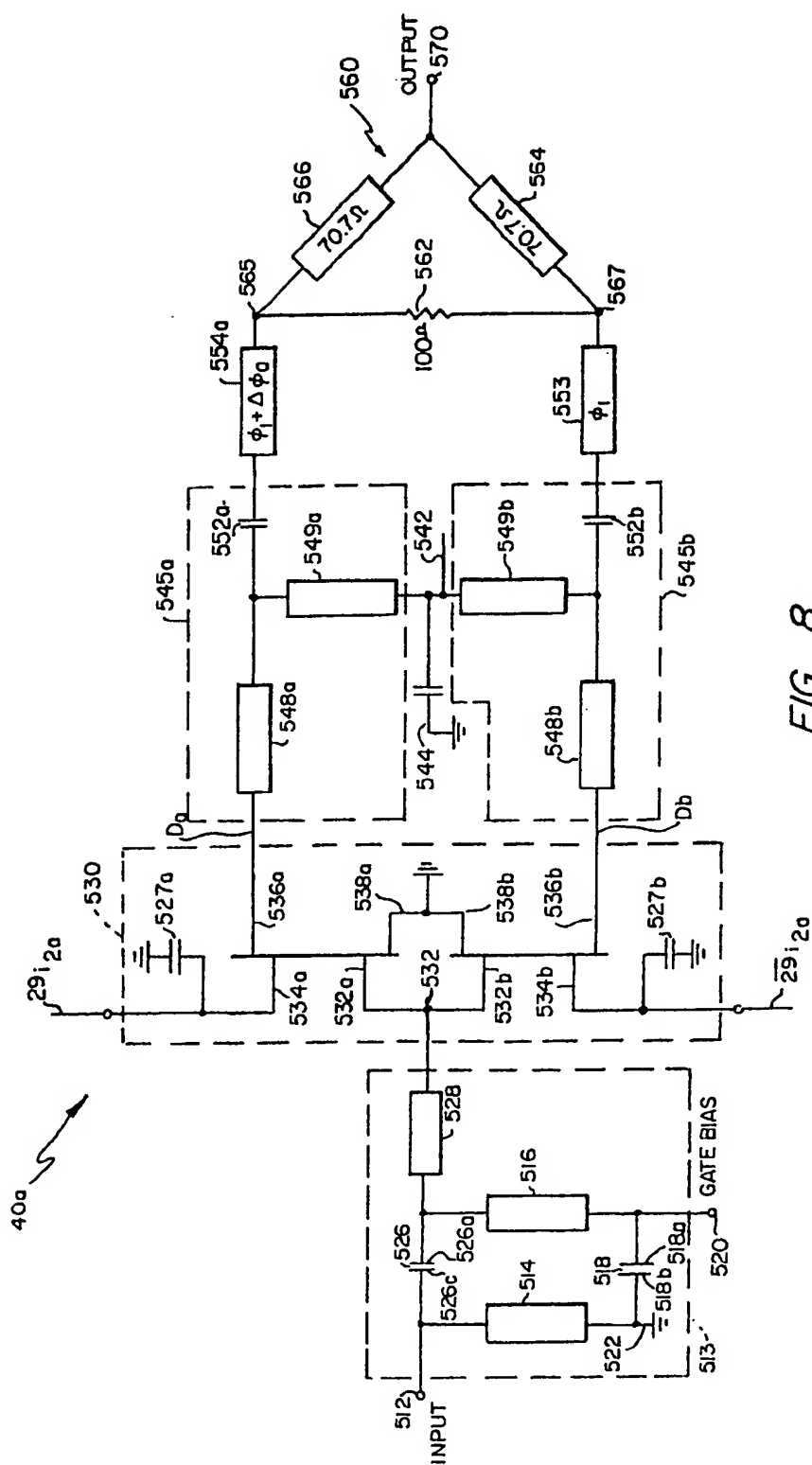

FIG. 8

FIG. 9A

FIG.9B

FIG.9C

FIG.9D

FIG. 11

FIG. 10

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FIG. 12

FIG. 13

FIG. 14

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FIG. 15

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FIG. 16

FIG. 17

FIG. 18

FIG. 19

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FIG.20
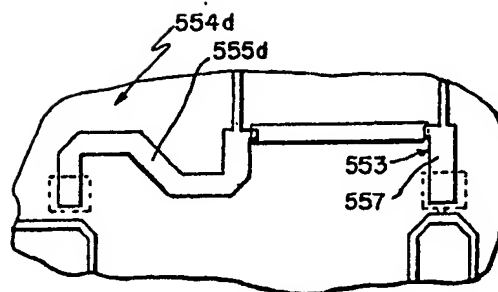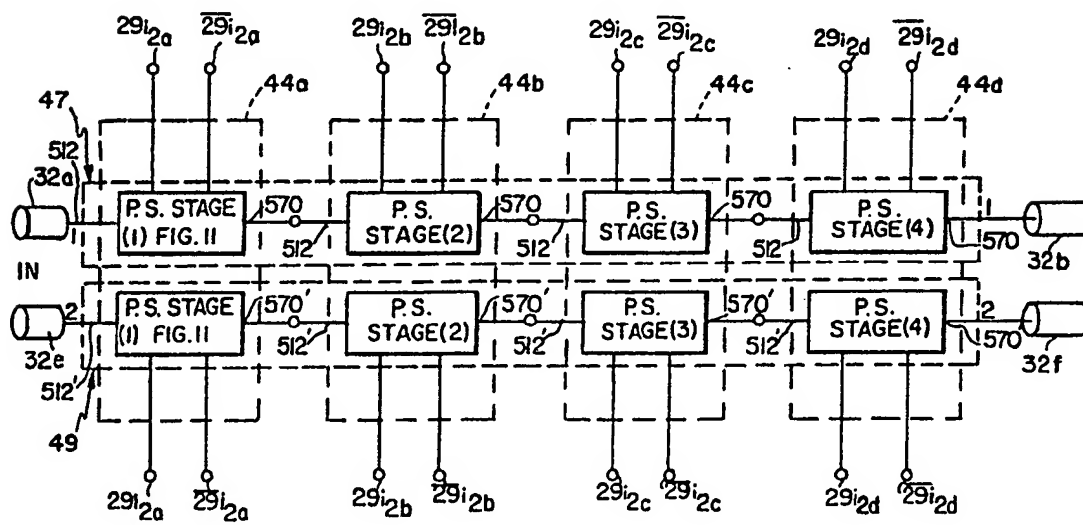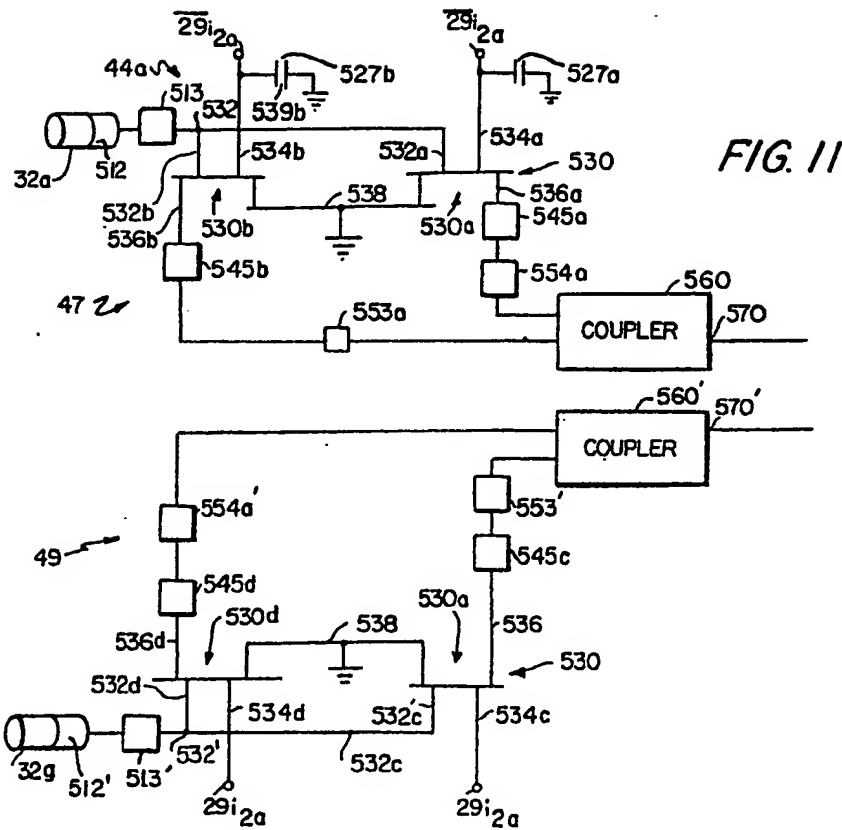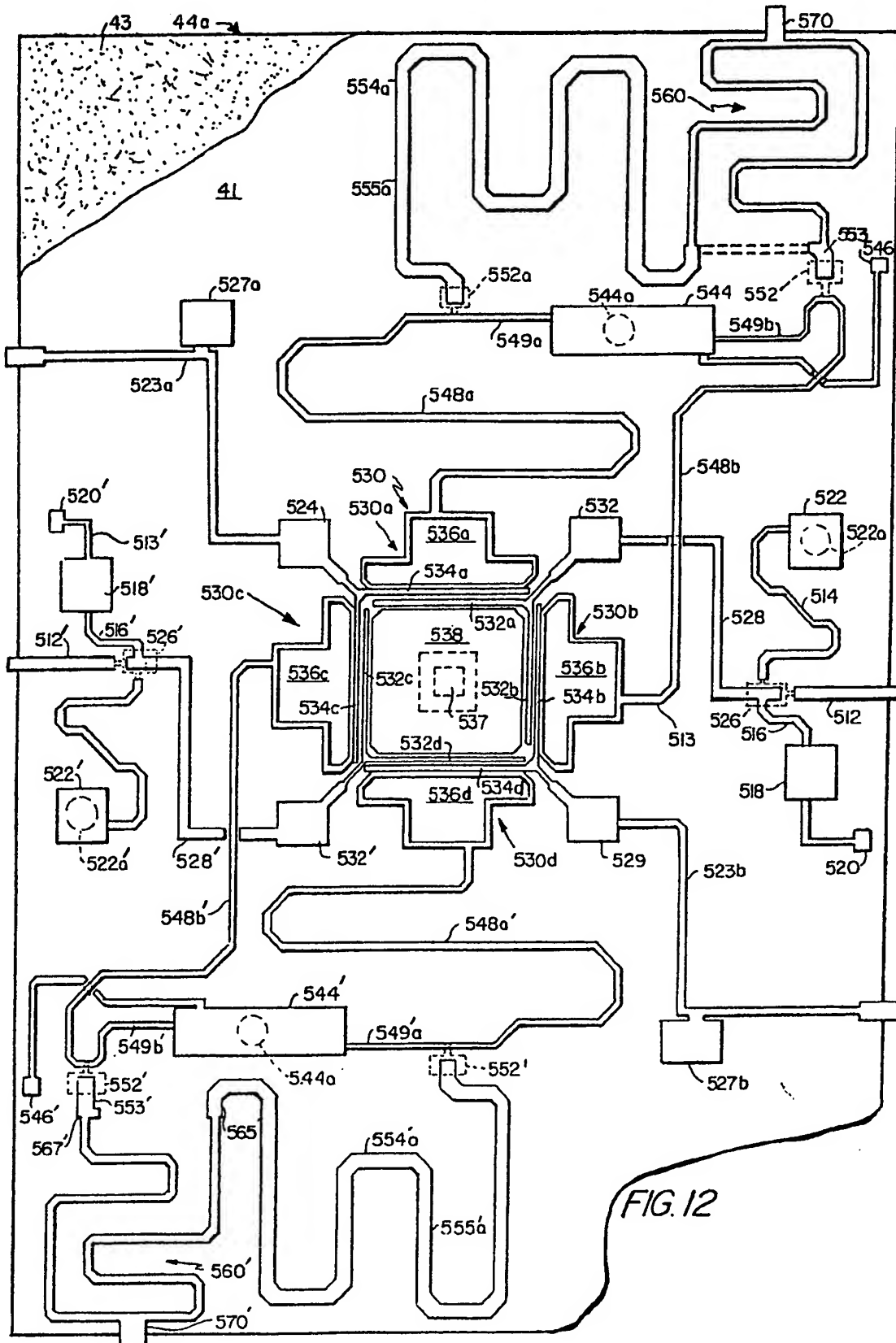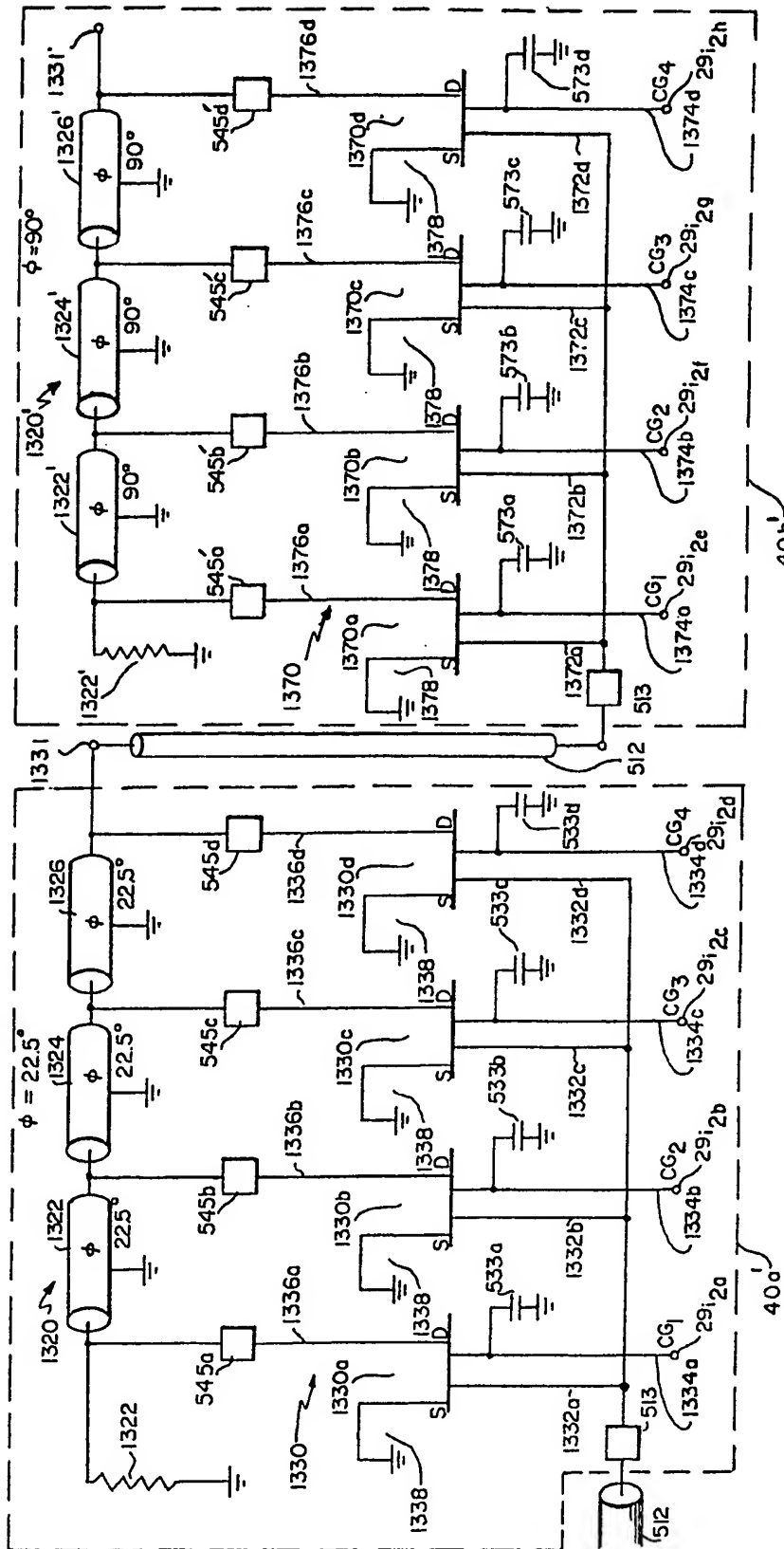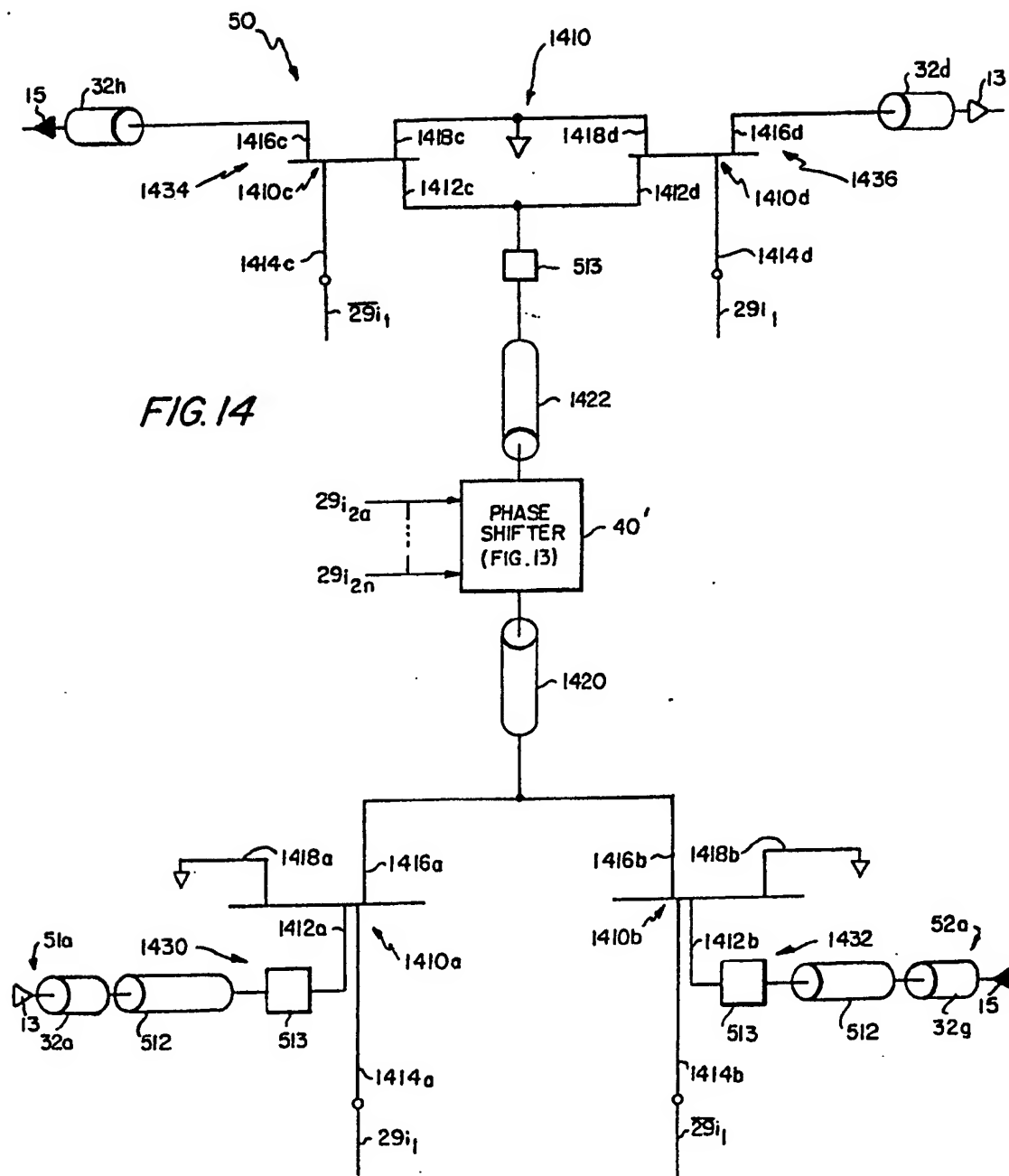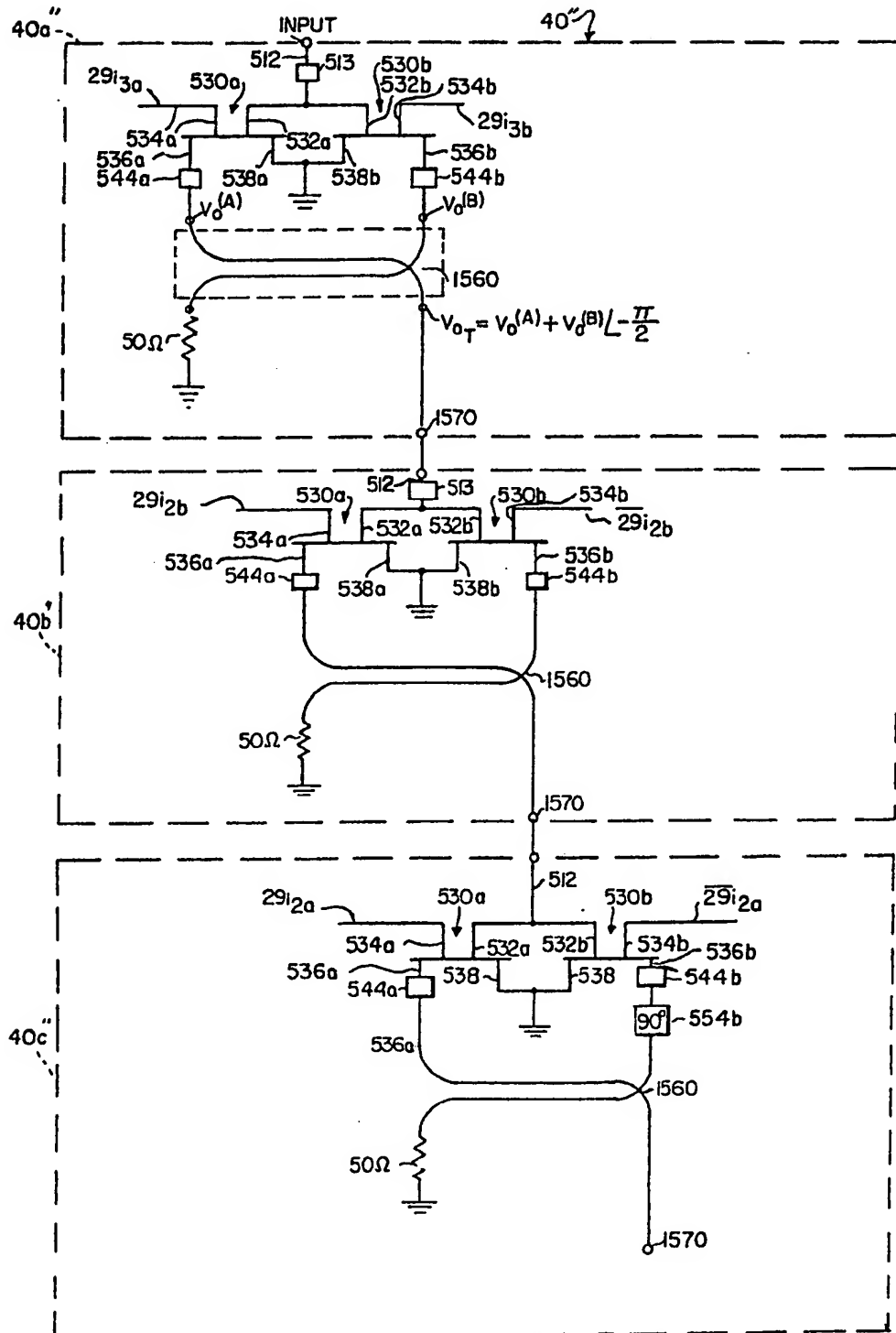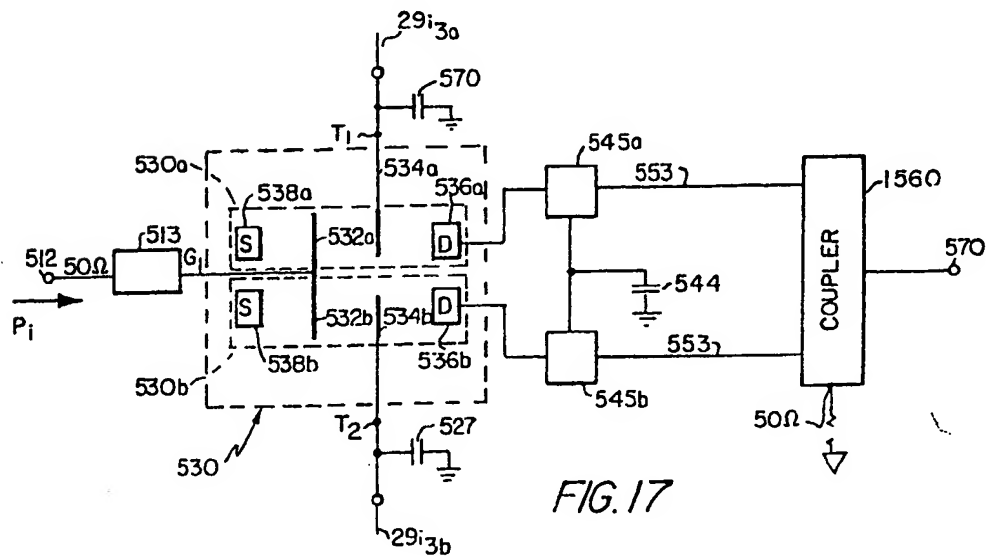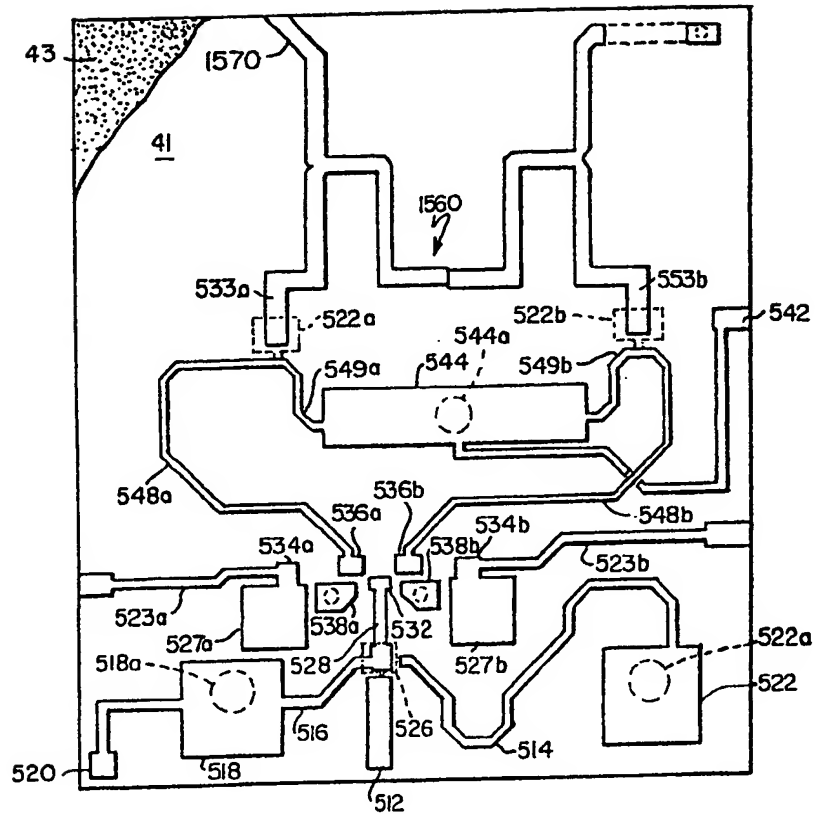
SPECIFICATION

Transceiv r el ment

5   This invention relates to antenna systems and more particularly to phased array antenna   5
systems.
       As is known in the art, an array antenna includes a plurality of individually radiating elements.
In some systems the individual radiating elements are coupled to a transmitter through a
transmitter element for controlling the phase and amplitude of the transmitted signal. Similarly,
10 the individual radiating elements are coupled to a receiver through a receiver element, for   10
controlling the phase and amplitude of the received signal. In other systems the individual
radiating elements are coupled to both the transmitter and receiver through a single element
here referred to as a transceiver for controlling the phase and amplitude of both transmitted and
received signals. The relative phase and amplitude of the microwave frequency signal passing
15 between the plurality of radiating elements and a corresponding plurality of individual tran-   15
sceiver elements are controlled to obtain a desired radiation pattern. The pattern obtained is a
result of the combined action of all the individual transceiver and radiating elements. Many
devices such as ferrite phase shifters are used to control the phase of the microwave frequency
signal. Many of such phase shifters are reciprocal, that is, the phase shift of a signal passing
20 through one of such devices is independent of the direction which the signal passes through. In   20
some applications it is desirable to provide an active phase shifter to provide gain to a signal
passing there through. Such a phase shifter is generally inherently nonreciprocal. Thus, the use
of an nonreciprocal phase shifter in a transceiver would require the use of two of such phase
shifters. A developing trend in phased array antenna systems is toward production of the
25 transceiver elements in monolithic integrated circuit form. This is desired in order to reduce cost   25
and size factors generally associated with phased array antenna systems and to provide phased
array antennas adapted for certain applications where size and cost are critical such as airborne
or space based radar systems.
       In accordance with the present invention, a transceiver for coupling a microwave signal
30 between an antenna element and a radar system, is provided. Such a transceiver includes a   30
plurality of switching means arranged to steer a microwave frequency signal provided by the
radar system through an nonreciprocal phase shifter to the phased array antenna during a
transmit mode, and to steer a microwave frequency signal provided from the phased array
antenna through the nonreciprocal phase shifter to the radar system during a receive mode. The
35 microwave frequency signal passes through the phase shifter in the same direction during both   35
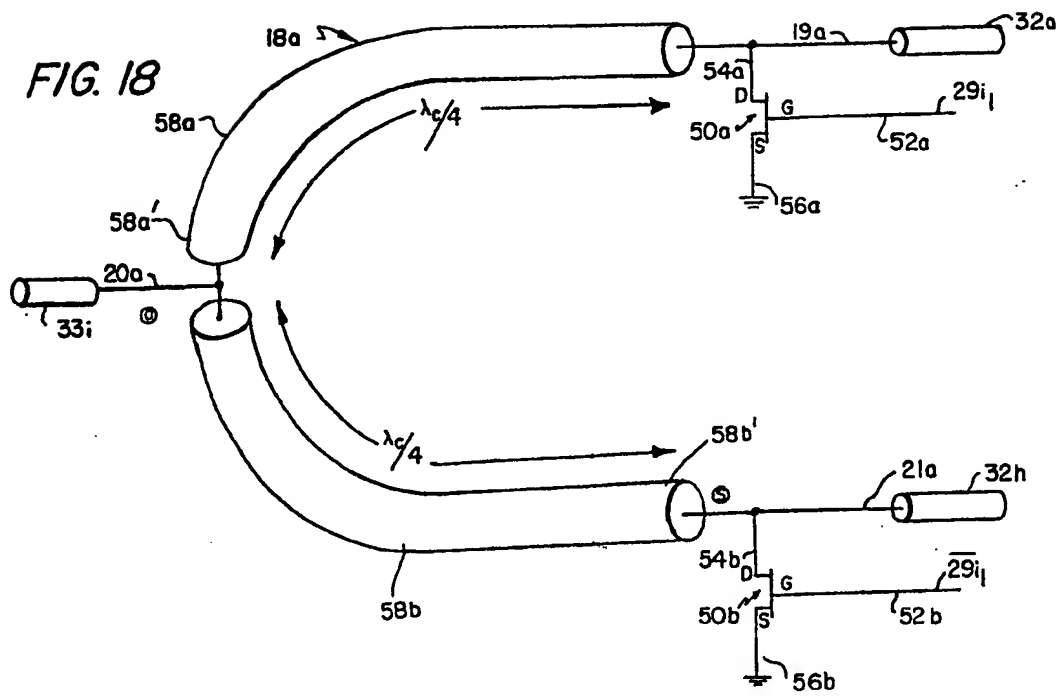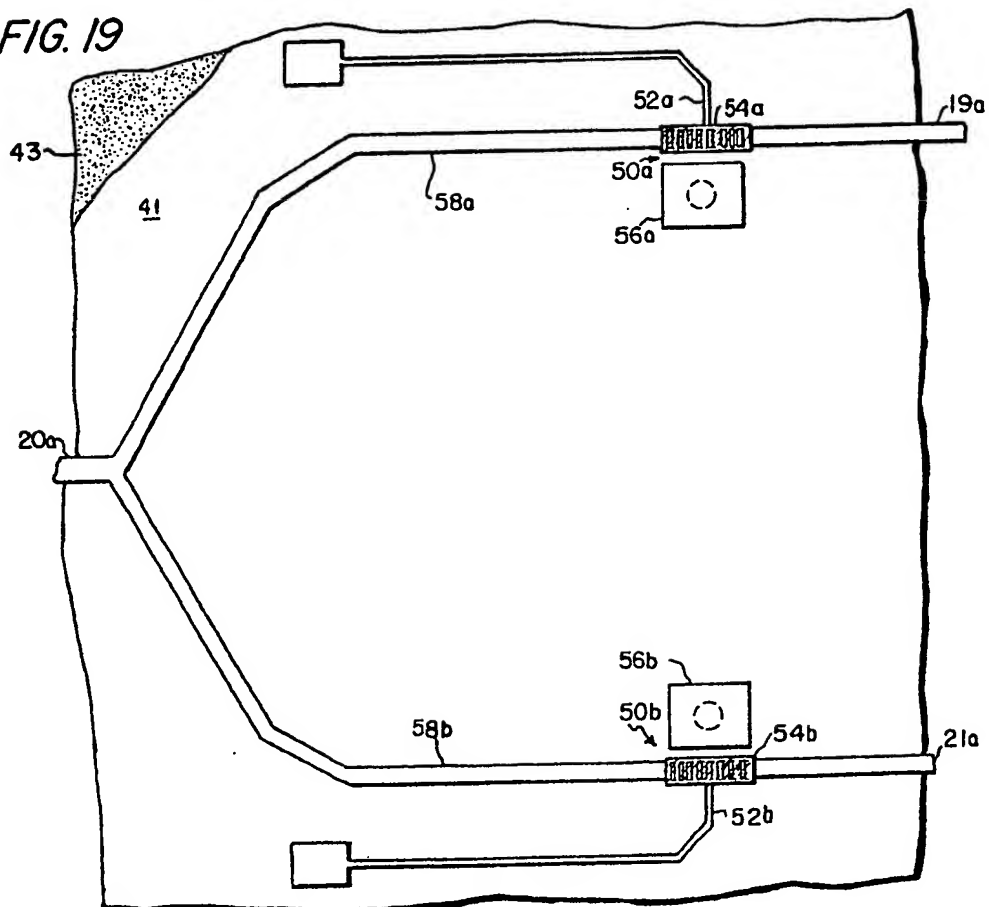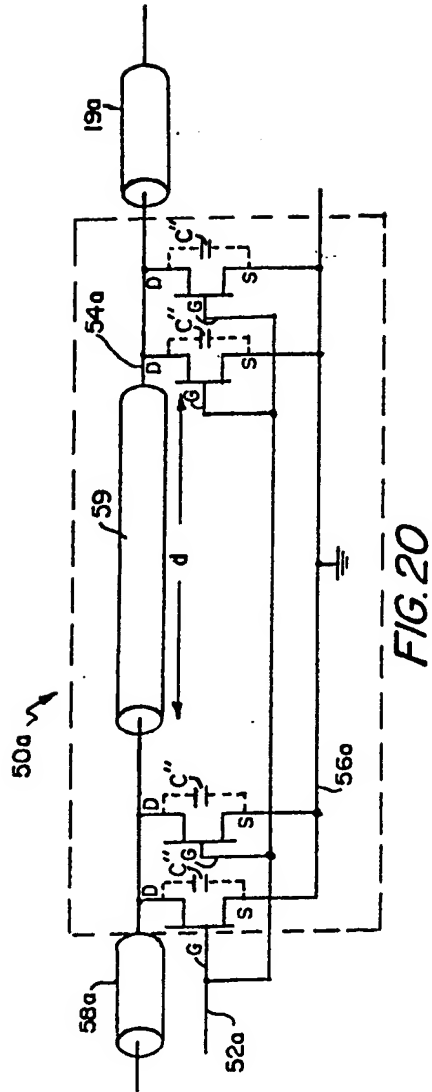the transmit and receive mode. A set of control signals is fed to such switching means to control
the steering of the microwave frequency signal between the radar system and the phased array
antenna. With such an arrangement, two signal paths through an active nonreciprocal phase
shifter are provided. This arrangement reduces the cost and size of the transceiver element by
40 permitting the use of a single active nonreciprocal phase shifter. Further, since each of the   40
elements of the transceiver element may be realized as monolithic microwave integrated circuits
this structure results in a compact transceiver element, modular in form and less expensive to
produce.
       The invention will now be described by way of example with reference to the accompanying
                                                                                                           45
45 drawings, in which:
       Figure 1 is an overall block diagram of a radar system coupled to a phased array antenna
system through a plurality of transceiver elements;
       Figure 2 is a block diagram of one of the plurality of transceiver elements shown in Fig. 1;
       Figure 3 is a block diagram of the transceiver element, utilizing a five port switch;
                                                                                                           50
50   Figure 4 is a block diagram of a transceiver using a dual channel phase shifter;
       Figure 5 is a block diagram of a 4-bit nonreciprocal phase shifter;
       Figure 6 is a diagrammatical view of a 180° phase shift increment stage of a 4-bit
nonreciprocal phase shifter used in the one of the transceiver elements;
       Figure 6A is an isometric view of a bias line and output line insulated from each other with an
                                                                                                           55
55 air gap plated overlay;
       Figure 6B is a cross sectional view of a parallel plat capacitor f rmed on the substrate;
       Figure 7 is a block diagram of th phase shifter stage depicted in Fig. 5;
       Figure 8 is a detailed schematic diagram of the phase shifter stage d picted in Fig. 5;
       Figures 9A–9D are plan views of pairs of transmission lines providing el ctrical pathlength
                                                                                                           60
60 differences used to r aliz a 4-bit phas shifter.
       Figure 10 is a block diagram of a 4-bit dual channel phase shifter;
       Figure 11 is a detailed schematic of on stage of a reciprocal phase shifter;
       Figure 12 is a diagrammatical vi w of the stage of a dual channel phase shifter depicted in
Fig. 11;
                                                                                                           65
65   Figure 13 is a detailed schematic of an alternate embodiment of a four bit nonr ciprocal

phase shifter;
   Figure 14 is a block diagram of the nonreciprocal phase shifter f Fig. 13, including reciprocating switches;
   Figure 15 is a detailed schematic diagram of a variable phase shifter utilizing a quadrature
5 coupler.   5
   Figure 16 is a plan view of the variable phase shifter shown in Fig. 15;
   Figure 17 is a block diagram of one stage of the n-bit variable phase shifter shown in Fig. 16;
   Figure 18 is a diagrammatical view of a bidirectional three port switch;
   Figure 19 is a schematic diagram of the bidirectional switch shown in Fig. 18;
10   *Figure 20* is a schematic diagram of a preferred field effect transistor FET used in the   10
bidirectional switch of Fig. 18.
   Referring now to Fig. 1, a phased array antenna 10 is coupled to a radar system 11 by a feed
network 14, as shown. The phased array antenna 10 includes a plurality of, here n, identical
transmitter/receiver (transceiver) elements 12a–12n, coupled to a like plurality of corresponding
15 antenna elements 26a–26n, as shown. The feed network 14, here a parallel feed network,   15
provides a signal path for a microwave signal passing from the radar system 11 to the phased
array antenna 10 for transmission to a target (not shown), and a signal path for reception of
echo signals from the target (not shown) to the radar system 11. A plurality of control buses
$29a–29n$, $\overline{29a}–\overline{29n}$ are provided from the radar system 11. Signals on such buses 29a–29n,
20 $\overline{29a}–\overline{29n}$ are used to control the transceiver elements 12a–12n of the phase array antenna 10.   20
The microwave signal from the feed network 14 is coupled to each of the transceiver elements
12a–12n, as indicated by the open arrows 13. The portion of microwave signal coupled to each
one of the transceiver elements 12a–12n is then coupled to the corresponding one of the
antenna elements 26a–26n. Similarly, a portion of the microwave echo signal from the target is
25 coupled to each of the antenna elements 26a–26n, the corresponding transceiver elements   25
12a–12n, and the feed network 14 as indicated by solid arrows 15, for processing by the radar
system 11. The control signals on buses 29a–29n, $\overline{29a}–\overline{29n}$ during the transmit mode allow
the transceiver elements 26a–26n to produce collimated and directed beams of transmitted
microwave energy and control signals on such buses during the receive mode allow such
30 transceiver elements 26a–26n to produce collimated and directed beams of received microwave   30
energy.
   Referring now to Fig. 2, a representative one of the transceiver elements 12a–12n, here
transceiver element 12i is shown coupled, via a transmission line 33i, to a portion of the feed
network 14 and to an antenna element 26i, via a transmission line 35i, as shown. Transceiver
35 element 12i here includes 50 ohm transmission lines 32a to 32h, four transmitter/receiver   35
(T/R) switches 18a–18d, each having a common port 20a–20d, a pair of branch ports
19a–19d and 21a–21d, and a control input 22a–22d. Each one of the control inputs 22a–22d
is fed by a pair of control lines $29i_1$, $\overline{29i}_1$ of buses 29i, $\overline{29i}$. The T/R switches 18a–18d are
here of a type to be further explained in conjunction with Figs. 18–19. Suffice it to say here,
40 however, that complementary, binary or logical signals are fed to the control lines $29i_1$, $\overline{29i}_1$,   40
respectively, and such logical signals are used to control the electrical coupling between the
common port and the branch ports. Thus, for example, using an exemplary one of the T/R
switches 18a–18d, here T/R switch 18a, such switch 18a has common port 20a coupled to
branch port 19a in response to a first pair of logical states of control signals fed to lines $29i_1$,
45 $\overline{29i}_1$ i.e. a logigal 1 on line $29i_1$ and a logical 0 on line $\overline{29i}_1$ and such common port 20a is   45
coupled to branch port 21a in response to the complementary pair of logical states of the
- control signals fed to line $29i_1$, $\overline{29i}_1$, i.e. a logical 0 on line $29i_1$ and a logical 1 on line $\overline{29i}_1$.
The common port 20a of T/R switch 18a is coupled to the feed network 14, via the
transmission line 33i, as shown. Branch ports 19a and 21a of T/R switch 18a are coupled to
50 branch ports 19d and 21b, via transmission lines 32a and 32h, respectively. Branch port 19b   50
of T/R switch 18b is coupled to an input of a transmitter amplifier 24, via the transmission line
32d. The transmitter amplifier 24 is here formed on a semi-insulating substrate, here a gallium
arsenide (GaAs) substrate. The output of transmitter amplifier 24 is coupled to the branch port
19c of T/R switch 18c, via transmission line 32e. The common port 20c of T/R switch 18c is
55 coupled to the antenna element 26i, via transmission line 35i. The branch port 21c of T/R   55
switch 18c is coupled to an input of the receiver amplifier 28, via transmission line 32f. The
receiver amplifier 28, here a low noise amplifier, is here formed on a semi-insulating substrate
(here GaAs). The output of the receiver amplifier 28 is coupled to the branch port 21d of T/R
switch 18d, via transmission line 32g. The common port 20d of T/R switch 18d is coupled to
60 the input of an active phase shifter 40, here a nonreciprocal active phase shifter having a   60
plurality of stages (n t shown, to be d scribed in detail in connection with Figs. 5, 6 and 7), via
transmission line 32b. Suffice it to say here, however, that each stage of the active phase shifter
includes a field effect transistor suitably biased to provide gain to the radio frequency signal
passing through it. Control signals for the active phase shifter 40 are fed thereto, via buses $29i_2$,
65 $\overline{29i}_2$ of bus 29i. The output of the active phase shifter 40 is coupled to the common port 23b of   65

T/R switch 18b, via transmission line 32c.

During a transmit mod , the transceiver element 12i couples a microwave frequency signal from the radar system 11 to the antenna element 26i. A transmit signal path for coupling a signal from the radar system 11, via feed network 14, to the antenna element 26i is depicted in
5   Fig. 2 by an open arrow 13, as shown. In the transmit mode, the control signals on lines $29i_1$, $\overline{29}i_1$ are used to couple each one of the common ports 20a–20d to the corresponding branch ports 19a–19d of the respective T/R switches 18a–18d. Thus a portion of the microwave signal is coupled from the radar system 11 to the input of the active phase shifter 40. The active phase shifter 40 is here used to vary the phase shift of the applied microwave frequency
10 signal by a predetermined amount in accordance with control signals on buses $29i_2$–$\overline{29}i_2$ which are fed to a control input 42, of the active phase shifter 40. The microwave frequency phase shifted signal is then coupled to the input of the transmitter amplifier 24. The signal at the output of the transmitter amplifier 24 is coupled to the antenna element 26i.

During a receive mode, a portion of a received echo signal is coupled from the antenna
15 element 26i to the radar system 11. A receive signal path for coupling the received echo signal from the antenna element 26i to the radar system 11 is depicted in Fig. 2 by solid arrows 15, as shown. During the receive mode the complementary logical states of the control signals previously on lines $29i_1$–$\overline{29}i_1$ are now fed to lines $29i_1$, $\overline{29}i_1$, and such signals are used to couple each one of the common ports 20a–20d to the branch ports 21a–21d of the respective
20 T/R switches 18a–18d. Thus the echo signal is coupled from the antenna element 26i to the receiver amplifier 28. The signal at the output of the receiver amplifier 28 is coupled to the input of the active phase shifter element 40. The signal passing through the phase shifter is again phase shifted in accordance with the control signals fed on buses $29i_2$–$29i_2$. The phase shifted signal produced at the output of the active phase shifter element 40 is then coupled to
25 the radar system 11, via the feed network 14. Thus is is noted that the microwave frequency signal is coupled through the active phase shifter 40 in the same direction for both the transmit mode and the received mode. Thus, referring again to Fig. 1 in a similar manner, each of the plurality of transceiver elements 12a–12n are used to couple a portion of microwave signal between the radar system 11, via the feed network 14 and the plurality of antenna elements
30 26a–26n, to produce in combination a collimated and directed beam (not shown) during the transmit mode and the receive mode.

Referring now to Fig. 3 an alternative the embodiment of a transceiver element 12i′ suitable for use in the phased array antenna 10 of Fig. 1 is shown coupled to a portion of the feed network 14 and the antenna elements 26i. Transceiver element 12i′ here includes a five port
35 switch 310, the active phase shifter 40, the transmitter amplifier 24, the receiver amplifier 28, and the three port T/R switch 18c, as shown. The five port switch 310 is formed on a substrate, (not shown) here semi-insulating gallium arsenide (GaAs) having a ground plane (not shown) here plated gold formed on the bottom surface of the substrate. Formed in active regions on portions of the top surface of the semi-insulating substrate are FET's 50a–50d here
40 GaAs FETs, each having gate electrodes 52a–52d (Fig. 3), a drain electrode 54a–54d and a source electrode 56a–56d. The gate electrodes 52a, 52d of FET's 50a, 50d, are connected to control line $29i_1$, and the gate electrodes 52b, 52c of FET's 50b, 50c are connected to control line $\overline{29}i_1$, as shown. The FET's are here connected in a common (grounded) source configuration. The T/R switch 310 further includes transmission lines 60a–60f. Each transmission line
45 60a–60f has an electrical length, corresponding to one quarter wavelength ($\lambda_c/4$), where λ_c is the wavelength of the corresponding nominal or operating centerband frequency (f_c) of the circuit. The feed network 14 is electrically connected to a first end 60_{a1} of $\lambda_2/4$ transmission line 60a and a first end $60f_1$ of $\lambda_c/4$ transmission line 60f, via transmission line 33i. The drain electrode 54c of FET 50c is electrically connected to a second end $60a_2$ of $\lambda_c/4$ transmission
50 line 60a. A first end $60b_1$ of $\lambda_c/4$ transmission line 60b is electrically connected to the second end $60a_2$ of transmission line 60a and drain electrode 54c. A second end $60b_2$ of $\lambda_c/4$ transmission line 60b is electrically connected to the input port of the active phase shifter 40, via transmission line 32b and to a first end $60d_1$ of $\lambda_c/4$ transmission line 60d. The second end $60d_2$ of transmission line 60d is electrically connected to the output of the recevier amplifier 28
55 and to the drain electrode 54d of FET 50d. A second end $60f_2$ of $\lambda_c/4$ transmission line 60f is electrically c nnected to a first nd $60e_1$ of $\lambda_c/4$ transmission line 60e, and drain electrode 54a of FET 50a. A second end $60e_2$ of $\lambda_c/4$ transmission lin 60e is coupl d to the output of the active phase shifter 40, via transmission line 32c and to a first end $60c_1$ of $\lambda_c/4$ transmission line 60c. A s cond end $60c_2$ f $\lambda_c/4$ transmission line 60c is coupled to the input f the
60 transmitter amplifier 24 and to the drain l ctrod 54b f FET 50b. The connections of transmitter amplifier 24 and receiver amplifier 28 to T/R switch 18d are the same, as xplained above in conjunction with Fig. 2.

During the transmit mod , as shown by the open arrows 13 a logical control signal on line $29i_1$ of bus 29i is fed to the gate electrodes 52a, 52d of FETs 50a, 50d and the complement of
65 such logical control signal is fed (via line $\overline{29}i_1$ of bus $\overline{29}i$) to gates 52b, 52c of FETs 50b, 50c.

In response to such signals FET's 50a, 50b are placed in a conducting state and FET's 50b, 50c are placed in a nonconducting state. Th $\lambda_c/4$ transmission lines 60d, 60e and 60f have ends $60d_2$, $60e_1$ and $60f_2$ electrically connected to FET's 50a and 50b, as pr viously described. When FET's 50a, 50d are placed in a conducting state, a short circuit (low impedance path to
5   ground designated by ⓢ) is produced at the ends $60d_2$, $60e_1$ and $60f_2$ of transmission lines 60d–60f coupled to the FET's 50a, 50d. One quarter wavelength therefrom (at the second end $60d_1$, $60e_2$, and $60f_1$ of each transmission line 60d–60f) the short circuits at ends $60d_2$, $60e_1$, $60f_2$ appear as open circuits (high impedance paths to ground designated by ⓞ) at ends $60d_1$, $60e_2$, $60f_1$, to a microwave frequency signal having a wavelength substantially equal to the
10 wavelength of the corresponding nominal or centerband frequency of operation, for the transceiver. Thus, no signal path is provided during the transmit mode through line 60f and the transmitted energy passes through lines 60a and 60b. Further because end $60d_1$ appears as an open circuit ⓞ, the transmitted energy passes from line 60b through line 32b, through the phase shifter 40 and through line 32c. Since end $60e_2$ appears as an open circuit ⓞ the
15 transmitted, and now phase shifted energy passes through line 60c, transmitter amplifier 24, T/R switch 18c and to the antenna 26i, as previously described in conjunction with Fig. 2.

During the receive mode as shown by the closed arrows 15, the control signals on lines $29i_1$, $\overline{29i_1}$ are switched (or complemented) in logic state placing FET's 50a and 50d in a nonconducting state, and placing FET's 50b and 50c in a conducting state. The ends $60a_2$,
20 $60b_1$, and $60c_2$ of the $\lambda_c/4$ transmission lines 60a, 60b and 60c which are coupled to the drain electrodes 54b and 54c of FET's 50b and 50d are thus coupled to ground and the other ends $60a_1$, $60b_2$, and $60c_1$ of the transmission lines 60a, 60b, and 60c present impedances corresponding to open circuits. Thus, a received microwave signal from antenna element 26i is coupled to the output of the receiver amplifier 28 as explained in conjunction with Fig. 2. The
25 received signal is then coupled through transmission line 60d to the active phase shifter element 40. The signal on the output of the active phase shifter 40 is thus coupled to the radar system 10 through transmission lines 60e and 60f.

Referring now to Fig. 4, an alternative embodiment of a transceiver, here transceiver 12i″ suitable for use in the phased array antenna 10 of Fig. 1 is shown coupled to a portion of the
30 feed network 14, via transmission line 33i and to the antenna element 26i, via transmission line 35i, as shown. Transceiver element 12i″ includes T/R switches 18a and 18c, transmitter amplifier 24, receiver amplifier 28. Here, however, a dual channel active phase shifter 44 is provided. Dual channel active phase shifter 44 has a plurality of cascade interconnected phase shift stages here 44a–44d of a type to be further described in detail in conjunction with Figs.
35 10–12. The T/R switch 18a has common port 20a coupled to the feed network 14 via transmission line 33i. Branch ports 19a and 21a of T/R switch 18a are coupled to the input 47a of a first channel 47 and the output 49b of a second channel 49 of dual channel phase shifter 44, respctively, as indicated. The output 47b of the first channel 47 is coupled to the input of the transmitter amplifier 24, via transmission line 32b. The output of the receiver
40 amplifier 28 is coupled to the input 49a of the second channel 49, via transmission line 32e. The connection of the transceiver 12i″ to antenna element 26i (Fig.1) is as previously explained.

During the transmit mode, as shown by the open arrows 13, in response to complementary control signals on lines $29i_1$, $\overline{29i_1}$ a microwave signal fed to common port 20a from the radar
45 system 11 is coupled to branch port 19a. Such signal from branch port 19a is coupled to the input 47a of the dual channel phase shifter 44. The signal is shifted in phase and coupled to the transmitter amplifier 24 and to the antenna 26, as previously described. During a receive mode, as shown by the closed arrows 15, in response to the complements of the previous control signals on lines $29i_1$, $\overline{29i}$ the microwave signal fed to the common port 20c from
50 antenna 26i is coupled to the branch port 21c and thus to the receiver amplifier 28. The signal at the output of the receiver amplifier 28 is fed to the input 49a of the phase shifter 44. The signal shifted in phase is then fed to the T/R switch 18a to the radar system 11, as previously described.

Referring now to Fig. 5, a single channel digitally controlled phase shifter 40 suitable for use
55 in transceiver element 12i (Fig. 2) and transceiver element 12i′ (Fig. 3) is shown to include a plurality of cascad interconnected stages 40a–40d with like parts of each stage being designated by the same numeral. An exemplary one of such stages 40a–40d, here stage 40a, is discussed in d tail in conjunction with Figs. 6–8. Referring now t Fig. 6, the phase shift r stage 40a is formed on a substrate 41 here GaAs having a ground plane 43, as shown.
60 Referring also to Figs. 7, 8 the phase shift r stage 40a includes a microwave transmission lin 512, here having an imp danc of 50 ohms, coupled to an input impedance matching circuit 513. Transmission line 512 is here fed by a microwav fr qu ncy signal from transmission lin 32b (Fig. 2). Input impedance matching circuit 513 is here used to match the input impedance of the phase shifter stage 40a to the characteristic impedance of the transmission line 512. The
65 input matching circuit 513, here includes a first transmission line section 514, having a

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reactance which is primarily inductive, coupled in shunt to the input transmission line s ction
512, via a bottom plate 526c of a capacitor 526. Bottom plate 526c of capacitor 526 is
coupled to one nd of th shunt mounted transmission line section 514. The upper plate 518a
of a second series connected capacitor 518 is coupled to line 516 and the bottom plate of 518
5 is coupled to ground by a via hole 518b, as shown. Ground pad 522 is coupled to ground by a   5
via hole connection 522a. As shown in Fig. 6B, capacitor 526 is formed on the top surface of
the substrate 41 here includes a top plate 526a which is coupled via an air bridge 526d to the
strip conductor portion of a transmission line 528. Aligned under this top plate is a bottom plate
526c of evaporated gold formed on the substrate 41. The top plate 526a and bottom plated
10 526c are separated by a 5000 Angstrom (A) layer 526b of silicon nitride (Si_3N_4). The bottom   10
plate 526c has a finger 526e (Fig. 6) which is used to connect the second circuit element, here
transmission line section 514, to the capacitor 526. The connection is provided by a metal to
metal contact which couples to the bottom plate 526c. A second transmission line section 516,
here having a reactance which is primarily inductive is coupled in shunt between capacitors 518
15 and 526. The connection of capacitor 518 to inductor section 516 provides the bias feed 520   15
for the gate electrode. The input matching circuit 513 further includes the third transmission
line section 528 here also having a reactance which is primarily inductive, connected between
the junction of capacitor 526 with shunt mounted transmission line section 516 and a common
input junction 532. The phase shifter stage 40a further includes a FET switch 530 having a
20 dual gate FET, 530a–530b, as shown. FET's 530a and 530b include first gate electrodes   20
532a–532b coupled to the common junction 532, second gate electrodes 534a, 534b,
separate drain electrodes 536a, 536b and separate source electrodes 538a, 538b. FETs 530a,
530b are here connected in a common (grounded) source configuration. FET 530a, 530b are
fabricated such that the gains and phases provided by each FET to signals fed to the gate
25 electrode and coupled to the drain electrode are substantially equal. In other words, $|S_{21}|_a$, the   25
fraction of power coupled to the drain electrode 536a of 530a from a signal on gate electrode
532a substantially equals, $|S_{21}|_b$, the fraction of power available at the drain electrode 536b of
FET 530b from an incident input signal provided signal gate electrode 532b of FET 530b.
Similarily, $\psi S_{21}|_a = \psi S_{21}|_b$ that is, the phases of the instantaneous power delivered to each drain
30 electrode of FET 530a, 530b are substantially equal. Control gate electrodes 534a, 534b are   30
fed control signals on lines $29i_{2a}$, $\overline{29i_{2a}}$ (Fig. 2). These control signals are used to control the
coupling of an input signal fed to the gate electrode 532a, 532b to the corresponding drains
536a, 536b of FET's 530a, 530b. High frequency components in the signals on control lines
$29i_{2a}$, $\overline{29i_{2a}}$ are shorted to ground, via capacitors 527a, 527b. The drain electrodes 536a, 536b
35 are electrically connected to identical impedance matching circuits 545a–545b, as shown. The   35
matching circuit 545a (Fig. 8), here includes a first transmission line section 548a coupled in
series between the drain electrode 536a and a coupling capacitor 552a. A second transmission
line section 549a is coupled in shunt with the junction of the first transmission line section
548a, the bottom plate of capacitor 552a, and an upper plate of a dc blocking capacitor 544.
40 The bottom plate of the dc blocking capacitor 544 is connected to ground by a via hole   40
connection 544a (Fig. 6). The impedance matching circuit 545b is formed in a similar manner
on the substrate 41 (Fig. 6) for the drain electrode 536b. The impedance matching circuit 545b
includes a transmission line section 548b, a coupling capacitor 552b, and a second transmis-
sion line section 549b, coupled to the drain electrode 536b in a similar manner as the
45 corresponding elements of impedance matching circuit 545a. The common connection of   45
transmission line sections 549a–549b and the dc blocking capacitor 544 provides the bias feed
546 for drain electrodes 536a, 536b. As shown in Fig. 6A, the bias feed 542 here is insulated
from the transmission line section 548b by a conventional air gap plated overlay. In general,
such overlays are here used in all embodiments to insulate such crossing signal paths. The
50 upper plates of coupling capacitors 552a–552b of the impedance matching circuits 545a,   50
545b respectively, are integrally formed with the strip conductor portion of transmission lines
554a and 553, respectively. Transmission line 554a has an electrical length which provides a
phase shift $\phi_1 + \Delta\phi_a$ to an input signal coupled thereto and transmission line 553 has an
electrical length which provides a phase shift of ϕ_1 to an input signal coupled thereto. Such pair
55 of transmission lines 554a, 553 as shown in Fig. 9a and described in more detail hereinafter   55
provides one path having an unique phase shift increment $\Delta\phi_a$. Each s cond end of transmission
line s ction 554a, 553 is coupled t a corresponding input port 565, 567 of a conventional
three port coupler, which couples power from two input ports and provides th coupled power
to an output port, via branch arms 564, 566. Such a coupler is described in an article entitled
60 "GaAs Monolithic Lange and Wilkinson Coupl rs" by Raymond C. Waterman Jr. et al, IEEE   60
Transactions on Electron Devices, Vol. ED–28, No. 2, February 1981. Th output of the thr e
port coupler is electrically connected to an output port 570. Capacitors 518, 526, 544, 552a,
552b, 527a and 527b are here formed in a similar manner, as explained for capacitor 526.
In operation, an input signal fed to transmission line 512 is coupled to ach gate electrode
65 532a, 532b. Such signal is coupled to one of the drain electrodes 536a, 536b selectively in   65

accordance with the control signals fed on lines $29i_{2a}$, $\overline{29}i_{2a}$ to the control gate electrodes 534a, 534b. If the input signal in response to such control signals on lines $29i_{2a}$, $\overline{29}i_{2a}$ is coupled to drain electrode 536a, the phase of such signal is shifted by an amount $\phi_1 + \Delta\phi_a$ thr ugh transmission line 554a.

5   Conversely, the electrical path from drain electrode 536b to the coupler 560 provides a pathlength corresponding to a phase shift of ϕ_1. Thus, if in response to the control signals on lines $29i_{2a}$, $\overline{29}i_{2a}$, the input signal is coupled to drain electrode 536b, the phase of such signal at the output 570 is shifted by an amount of ϕ_1 through transmission line 553. Thus, a phase shift of an input signal of ϕ_1 or $\phi_1 + \Delta\phi_a$ at the output 570 is selected in response to control
10 signals on lines $29i_{2a}$, $\overline{29}i_{2a}$. A plurality of such stages are cascade interconnected to form the phase shifter 40 (Fig. 5). Each stage has two paths which correspond to phase shifts of an input signal of ϕ_1 through one path an amount $\phi_1 + \Delta\phi_i$ through the second path where i is the number of the stage. For, four cascade interconnected stages, the phase shift $\Delta\phi_i$ for each stage is here $\Delta\phi_a = 180°$, $\Delta\phi_b = 90°$, $\Delta\phi_c = 45°$ and $\Delta\phi_d = 22.5°$.

15   Referring again to Fig. 5, with like parts in each stage being designated by the same numeral, the active nonreciprocal phase shifter 40 used to produce an output signal at port 570d having a predetermined phase shift relative to an input signal on transmission line 512 includes four cascaded interconnected phase shifter stages 40a–40d, as shown. Each phase shifter stage 40a–40d realized in accordance with Fits. 6–8, selectively provides a unique phase shift to an
20 input signal of $\Delta\phi_a = 180°$, $\Delta\phi_b = 90°$, $\Delta\phi_c = 45°$ and $\Delta\phi_d = 22.5°$, respectively. Each phase shift stage includes a unique length of transmission line between output matching circuit 545a and the three port coupler 560. Each length of transmission line, in conjunction with the length of transmission line 553, provides each stage with a unique pathlength difference corresponding to the unique phase shift. In response to control signals on lines $29i_{2a}$–$29i_{2d}$, and $\overline{29}i_{2a}$–$\overline{29}i_{2d}$
25 selective combinations of phase shift increments of 0° or 180°, 0° or 90°, 0° or 45° and 0° or 22.5° are provided by phase shifter stages 40a–40d, respectively of control signals fed by lines $29i_{2a}$ to $29i_{2d}$ and $\overline{29}i_{2a}$ to $\overline{29}i_{2d}$ are represented by A to D and $\bar{A}$ to $\bar{D}$, respectively. The phase shift ϕ of an input signal through phase shifter 40 may be represented by the following logical equation as:

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$$\phi = [(A(\phi_1 + \Delta\phi_a) + \bar{A}(\phi_1)) + (B(\phi_1 + \Delta\phi_b) + \bar{B}(\phi_1)) + (C(\phi_1 + \Delta\phi_c) + \bar{C}(\phi_1)) + (D(\phi_1 + \Delta\phi_d) + \bar{D}(\phi_1)].$$

The phase shifter 40, thus, is used to vary the phase of a signal fed to transmission line 512 of stage 40a from 0 to 360° in here 22.5° phase shift increments.

Referring now to Figs. 9A–9D transmission line sections 553 and 554a–554d used to
35 provide unique incremental phase shifts for stages 40c–40d respectively, of the phase shifter 40b shown in Fig. 5, have like parts being designated by the same numeral. The transmission lines 553 and 554a–554d are coupled to the input ports 565, 567 of the three port coupler 560, having a thin film load resistor 562 and branch arms 564, 566, and to a portion of the impedance matching networks 545a–545b, as shown. The transmission lines 554a–554d are
40 formed on the semi-insulating substrate 41 by strip conductors 555a–555d and 557, respectively, and the ground plane 43, which is separated by a dielectric, here the semi-insulating substrate 41. Strip conductors 555a–555d and 557 are designed to provide the corresponding transmission lines 554a–554d and 553 each with a 50 ohm characteristics impedance. The transmission lines 554a–554d each have an electrical length equal to a
45 corresponding precise fractional wavelength $\lambda_c/2^n$, with respect to transmission line section 553, where λ_c is the wavelength of the nominal or centerband operating frequency (f_c) for the active phase shifter n is the total number of stages. Thus, transmission line section 554a has a pathlength ($\Delta\phi_a$) equal to $\lambda_c/2$ with respect to transmission line section 553. In a similar manner, the pathlengths for segments 554b–554d with respect to transmission line 553 are
50 $\lambda_c/4$, $\lambda_c/8$, and $\lambda_c/16$. Thus, the transmission lines 554a–554d, with respect to transmission line section 553, here represent path length differences corresponding to a phase shift of an applied signal with respect to the phase of such signal of 180°, 90°, 45° and 22.5°, respectively.

Referring now to Fig. 10, a dual channel phase shifter 44 having channels 47 and 49 which
55 is suitable for use in the transceiver 12i″ shows in Fig. 4 includes four one bit phase shifter stag s (P.S.Stages) 44a–44d cascade interconnected together, as shown, The dual channel phas shifter stages 44a–44d ar here identical except for th pathlength differences (phase shift increment) ($\Delta\phi_i$) forming the phase shift n tworks of each stage. Each chann l of the dual channel phase shifter provides one of two signal paths, such path being selected in response to
60 control signals fed on lines $29i_{2a}$–$29i_{2d}$ and $\overline{29}i_{2a}$–$\overline{29}i_{2d}$. Such paths provide either a phase shift of ϕ_1 or a phase shift of $\phi_1 + \Delta\phi_i$ where i is th number of the stage. The phase shift increment ($\Delta\phi_i$) for each of the four stages 44a–44d shown in Fig. 10 are a $= 180°$, $\Delta\phi_b = 90°$, $90°$, $\Delta\phi_c = 45°$ and $\Delta\phi_d = 22.5°$ for stages 44a–44d, respectively as explained in conjunction with Figs. 9a–9d.

65   Referring now to Fig. 11, an ex mplary one of such phase shifter stages, here phase shifter   65

stage 44a is shown. The phase shifter stage 44a includ s FET's 530a–530d each having a pair
of gate electrodes 532a–532d, and 534a–534d, a drain electrode 536a–536d, and a common
source electrode 538. FET's 530a–530d are here realized as a double pole double throw FET
switch 530 of a type disclosed in U.S. Patent No. 4,313,126 filed May 21, 1979, and
5 assigned to the assignee of this invention. Each of the FET's 530a–530d are here connected in   5
a common (grounded) source configuration, as shown. Each FET 530a–530d is formed on the
substrate 41 within close proximity to the other FET's 530a–530d, as shown. FETs
530a–530d are fabricated such that gains and phases provided to an input signal are
substantially equal, as explained in conjunction with Figs. 6–7.
10   The first phase shifter channel 47 includes a microwave transmission line 512, here coupled   10
to the transceiver 12i'' (Fig. 4), via transmission line 32a provided a signal input for the phase
shifter stage 44a. The microwave transmission line 512 is electrically connected to an
impedance matching circuit 513a previously described in conjunction with Figs. 6–8. Matching
circuit 513 is electrically connected to the common input junction 532. Input junction 532 is
15 coupled to input gate electrodes 532a, 532b of FET's 530a, 530b, respectively. Signals fed on   15
lines 29i_{2a}, $\overline{29}i_{2a}$ from the radar system 11 (Fig. 1) are fed to the second gate electrodes 534a,
534b for controlling the conduction of an input signal on input gate electrodes 532a, 532b to
the corresponding drain electrodes 536a, 536b of FET 530a, 530b, respectively. High
frequency signal components on control signals fed on lines 29i_{2a}, $\overline{29}i_{2a}$ are shorted to ground
20 by capacitors 527a, 527b. An input signal fed equally to input gate electrodes 532a, 532b is   20
selctively coupled, to the corresponding drain electrode 536a, 536b, in accordance with the
control signals on lines 29i_{2a}, $\overline{29}i_{2a}$ fed to the control gate electrodes 534a, 534b. The drain
electrodes 536a is electrically connected to an impedance matching network 545a as described
in conjunction with Figs. 5–7. The drain electrode 536b is similarly, electrically connected to
25 the impedance matching network 545b, as shown. The impedance matching network 545a is   25
coupled to here, the microwave transmission line 554a. In a similar manner, the impedance
matching network 545b is coupled to the microwave transmission line 553a. Each second end
of transmission lines 553a and 554a is coupled to the pair of input 565, 567 of the
conventional three port coupler 560.
30   The second channel 49 of digital phase shifter stage 44a includes microwave transmission   30
line 512' coupled to transceiver 12i'' (Fig. 4) via transmission line 32g (Fig. 2) for providing the
signal input for channel 49. The microwave transmission line 512' is electrically connected to
an impedance matching circuit 513' as previously disclosed in conjunction with Figs. 5–7. A
second matching circuit 513' is electrically connected to a common junction 532'. Common
35 junction 532' is electrically connected to input gate electrodes 532c, 532d of FET's 530c,   35
530d. Control gates 534c, 534d of FET 530c, 530d are electrically connected to gate electrode
pads 524 and 527, respectively. The control gates 534c, 534d are fed signals on lines 29i_{2a},
$\overline{29}i_{2a}$ from the radar system 11 (Fig. 1) for controlling conduction of an input signal on input
gate electrodes 532c, 532d to the drain electrodes 536c, 536d of FET's 530a, 530b,
40 respectively. Drain electrodes 536c–536d are electrically connected to impedance matching   40
networks 545c–545d as disclosed in conjunction with Figs. 6–8. Transmission lines 553' and
554a', are coupled between the impedance matching networks 545c–545d and the three port
coupler 560'. The three port coupler 560' is electrically connected to output port 570'.
    The total pathlength difference of the connection of drain electrode 536a to the three port
45 coupler 560, for channel 47 is then selected to provide a corresponding phase shift equal to   45
$\phi_1 + \Delta\phi_a$, as explained in conjunction with Figs. 9a–9d. The total pathlength difference of the
connection of drain electrode 536b to the three port coupler for channel 47 is selected to
provide a corresponding phase shift equal to ϕ_1. Thus, the phase of a signal applied to the gate
electrodes 532a, 532b is shifted by an amount $\phi_1 + \Delta\phi_a$ or ϕ_1 selectively in accordance with
50 control signals fed to control gate electrodes 534a, 534b. In the same manner, transmission   50
lines 553', 554a' provide pathlengths to channel 49 between drains 536c, 536d of $\phi_1 + \Delta\phi_a$ or
ϕ_1.
    Referring again to Fig. 10, the dual channel phase shifter 44 having channels 47 and 49 has
stages 44a–44d, each stage providing a unique phase shift to an applied signal. Each channel
55 provides selective combinations of phase shift increments $\Delta\phi_a = 180°, \Delta\phi_b = 90° \Delta\phi_c = 45°$, and   55
$\Delta\phi_d = 22.5°$ in response to control signals on lines 29i_{2a}–29i_{2d}, $\overline{29}i_{2a}$–$\overline{29}i_{2d}$.
    Referring now to Fig. 12, the phase shift r stage 44a is shown, formed on a semi-insulating
substrate 41 having a ground plane 43 on one side thereof, as shown. A low inductance ground
connection 537 is here made through the sourc electrode region 538. Parallel plate capacitors
60 such as 526 are formed on the substrate 41, as previously described in conjunction with Fig.   60
6B. Crossing signal paths are insulated one from another by conventional air gap plated overlays
as described in conjunction with Fig. 6A.
    Referring also to Fig. 5, the net overall gain for ach four bit phase shifter 40 and 44' is
approximately 8 decibels (db) or approximately 2db p r stage. Each stage contributes 3db of
65 loss from splitting of the input signal and an ther 3 db of loss due to power r combining at the   65

three port coupler 560. The total l sses due to parasitic losses and th matching n tworks are
less than 1 db. Allowing for substantial mismatch, a gain of approximately 8 db generally is
realizable from a dual gate FET, operating at X-band, for example. Thus, a net grain of
approximately 2 db per stage or approximately 8db for the phase shifters of Fig. 9 and Fig. 12
5 is realized. Since only four FETs, one per stage, at any given time are operating for each phase   5
shifter, 40, 44 the d.c. power consumption will be four times that for one FET.
    Now referring to Fig. 13, an alternative embodiment for a four bit digitally controlled phase
shifter 40' suitable for use in transceivers 12i and 12i' (Fig. 2 and Fig. 3) includes a first stage
40a' having a single pole four throw (SP4T) FET switch 1330 and a second stage 40b' having
10 an SP4T FET switch 1370, as shown. The SP4T FET switches 1330 and 1370 are here of a   10
type disclosed in the above mentioned U.S. Patent No. 4,313,126. Each stage 40a', 40b' is
formed on a substrate (not shown), having a ground plane (not shown).
    The first stage 40a' of the four bit digital phase shifter 40' further includes FET's
1330a–1330d, as shown, FET's 1330a–1330d are fabricated such that gains and phases
15 provided to an input signal are substantially equal, as explained in conjunction with Fig. 5–7.   15
Each FET 1330a–1330d, includes a input gate 1332a–1332d, a control gate 1334a–1334d,
drain electrodes 1336a–1336d and a source region 1338. FET's 1330a–1330d are here
connected to a common (grounded) source configuration. A low inductance ground connection
is here made from the source electrode 1338 to the ground plane 43 (not shown) by a
20 conventional via hole connection.   20
    A microwave transmission line 512, here having an impedance of 50 ohms is coupled to an
impedance matching circuit 513, as previously explained in conjunction with Figs. 4–6. The
impedance matching circuit is coupled to input gate electrodes 1332a–1332d. The drains
1336a–1336d are electrically connected to identical impedance matching networks
25 545a–545d of a type previously described in conjunction with Fig. 8. Impedance matching   25
networks 545a–545d are each coupled to a transmission line 1320 having a characteristic
impedance Z_o, here 50 ohms. Transmission line 1320 is terminated at one end in a resistor
1322, here having a value equal to 50 ohms, the characteristic impedance of the transmission
line 1320. The resistor 1322 is coupled in shunt between the transmission line 1320 and
30 ground. Drain electrode 1336d is electrically connected to the end of transmission line 1320   30
through the impedance matching network 545d. Drain 1336c of FET 1330c is electrically
connected to transmission line 1320, through the matching network 545c defining a section of
transmission line 1326, drain electrode 1336b of FET 1330b is electrically connected to
transmission line 1320 through the matching network 545b defining a section of transmission
35 line 1324, and drain electrode 1336a of FET 1330a is electrically connected to transmission   35
line 1320, through the matching network 545a, defining a section of transmission line 1322.
Here, all the transmission line sections 1322–1326 have the same electrical length and thus
each section shifts the phase of an applied signal by an equal amount. The total phase shift of
an output signal with respect to the phase of the input signal fed through transmission line 512
40 is the sum of the phase shifts provided by each of the equal electrical length transmission line   40
sections 1322, 1324 and 1326 of which the output signal passes through from a selected one
of the drain electrodes 1336a–1336d to the output port 1331.
    In operation, an input signal is coupled or decoupled between the gate electrodes
1332a–1332d and the corresponding drain electrode 1336a–1336d selectively in accordance
45 with control signals fed to control gate electrodes 1334a–1334d on lines $29i_{2a}$–$29i_{2d}$ provided   45
by suitable modification of the radar system 11 (Fig. 1). Signals on control lines $29i_{2a}$–$29i_{2d}$ are
here logical signals. One of such signals on lines $29i_{2a}$–$29i_{2d}$ is selected to be in an "on" state,
while the remaining ones of such signals on lines $29i_{2a}$–$29i_{2d}$ are placed in an "off" state, thus
placing only one FET of the FETs 1330a–1330d, in a conductive state and the remaining ones
50 of such FET's 1330a–1330d, in a non-conductive state. Similarly the output signal from the   50
first stage is coupled or decoupled between the gate electrodes 1372a–1372d and the
corresponding drain electrode 1376a–1376d selectively in response to control signals fed to
control gate electrodes 1374a–1374d, via lines $29i_{2e}$–$29i_{2h}$, as shown.
    In response to a control signal fed to one of the control gate electrodes 1334a–1334d the
55 corresponding one of the FET's 1330a–1330d is placed in a conducting state, coupling the   55
input signal on the input gat electrode of such FET, to th corresponding drain electrode of
such FET. The remaining FET's of th FET's 1330a–1330d ar held in a nonconducting state
by control signals fed to r maining ones of the control gates 1334a–1334d. Thus, a signal
coupled to the transmission line 1320 from drain electrode 1336a will have a net phase shift of
60 $3\Delta\phi$ with respect to phase of an input signal on drain electr de 1336a, because the signal   60
coupled from drain lectrode 1336a will pass through the three phase shift sections 1322,
1324 and 1326 of transmission line 1320 before arriving at the output port 1330. In a like
manner, a signal applied from the drain electrode 1336b to transmissi n line 1320 will hav a
net phase shift of $2\Delta\phi$, a signal applied from drain electrode 1331c to transmission line 1320
65 will have an incremental phase shift of $\Delta\phi$, and a signal applied from drain electrode 1336d to   65

transmission line 1320 will have an incremental phase shift of 0° with respect the signal on drain electrode 1336d. Thus by selective application of control signals fed to control gates 1334a–1334d an incremental phase shift of 3Δφ, 2Δφ,Δφ, or 0° may be obtained. By selecting the electrical length of each incremental phase shift (Δφ) of the first stage equal to b_ 22.5°, a
total phase shift of up to 67.5° is provided by the first stage. The phase shift provided by the matching network 545a–545d is the same for each drain electrode matching circuit and thus does not affect the differential phase shift produced.

The output of the first stage 40a′ is electrically connected to the input of the second stage 40b′, as shown. The second stage 40b′ of the four bit digital phase 40′ is identical to the first stage 40a′ except for the electrical length of the transmission line 1320′. In a like manner, as discussed for the first stage 40a′, the second stage of the four bit digital phase shifter 40′ has drain electrodes, here 1376a–1376d electrically connected to a portion of a transmission line 1320′. The incremental phase shift of transmission line 1320′ is here set to 90°. Thus, a total phase shift of·270° at the output 1331′ is obtainable in the second stage 40b′. This in
combination with the first stage 40a′ having a total available phase shift of 67.5° provides the four bit digital phase shifter 40′, having a capability of providing a·360′ phase shift, in 22.5° increments.

Now referring to Fig. 14, a digitally controlled phase shifter section 50 suitable for use in the transceiver 12i (Fig. 2), by replacing T/R switches 18b, 18d and phase shifter 40, and for
transceiver 12i″ (Fig. 4) by replacing phase shifter 44, includes the single channel phase shifter 40′ of Fig. 13, and FET's 1410a–1014d. Each FET 1410a–1014d has a signal gate electrode 1412a–1412d, a control gate electrode 1414a–1414d, drain electrodes 1416a–1415d, and source electrodes 1418a–1418d, as shown. FET's 1410a 1410d are connected in a common (grounded) source configuration. The signal gate electrodes 1412a, 1412b of FET's 1410a,
1410b are here coupled to the transmission lines 32a and 32g of the transceiver 12i (Fig. 2) respectively, through a pair of impedance matching circuits 513, as described in conjunction with Fig. 5. Each drain electrode 1416a, 1416b is coupled to the phase shifter 40′ via transmission line 1420. The output of the phase shifter 40′ is coupled to the input gate electrodes 1412c, 1412d of FET's 1410c, 1410d, respectively, via transmission line 1422 and
impedance matching circuit 513. The drain electrodes 1416c, 1416d are coupled to transmission lines 32h and 32d, respectively, of the transceiver 12i (Fig. 2). In operation, one of a pair of input signals fed to the signal gate electrodes 1412a, 1412b of input channels 1430, 1432 is selectively coupled to the corresponding drain electrodes 1416a, 1416b in response to signals fed to control gate electrodes 1414a, 1414b on lines 29i₁, 29̄i₁. Such selectively
coupled signal is fed to the phase shifter 40′ and the phase of such signal is shifted in response to control signals 29i₂ₐ–29i₂ₕ as previously described. One of the pair of output channels 1434, 1436 is selected, by signals on lines 29i₁, 29̄i₁ fed to control gates 1414c, 1414d. The phase shifted signal, is coupled to the input gate electrodes 1412c, 1412d of FETs 1410c, 1410d. The phase shifted signal fed to each of the input gate electrodes 1412c, 1412d is coupled to
one of the drain electrodes 1416c, 1416d selectively in response to control signals on lines 29i₁, 29̄i₁ fed to control gates 1414c, 1414d, respectively, as previously explained. The signal on the selected one of the drain electrodes 1416c, 1416d is coupled to transmission lines 32h during the receive mode or 32d of the transceiver 12i (Fig. 2) during the transmit mode.

Assuming one milliwatt of power consumption per FET, the power consumption of the phase
shifter 50 is four milliwatts since four FET's are conducting at the same time. Two FET's of the four reciprocating switches conduct and·one FET in each of stages 40a′ and 40b′ (Fig. 13) conducts, during operation of the phase shifter. The net overall gain for the phase shifter section 50 is approximately 4 db. This assumes a 6 db loss due to input signal division into the four channels, FET's 1330a–1330d of phase shifter stage 40a′ (Fig. 13) and 6 db of loss due to
input signal division for stage 40b′ (Fig. 13). In addition, there is a loss of 3 db in each stage (40a′, 40b′) attributable to the terminating resistors 1322 for transmission lines 1320 and 1320′ (Fig. 13), and there is a loss of 1 db per stage due to parasitics and the matching circuits. These losses are partially compensated for by a minimum of 8 db gain for each FET resulting in a net loss of at most 2 db per stage. Moreover, the FET switches 1410a–1410d
contribute 16 db of gain (8 bd per switch, two switches active at one time). This gain is reduced, however, by 3 db du to signal division into the two chann ls of FET's 1410a, 1410d and 1 db due to parasitics and the matching circuits. Thus, the net gain for the phas shifter 50 is approximately 4 db.

Referring now to Fig. 15, an alternative embodiment of an phase shifter 40″ suitable for use
in transceiver 12i (Fig. 2) and 12i′ (Fig. 3), includes a first phase shifter stage 40a″, a second phase shifter stage 40b″, and a third phase shifter stag 40c″ cascade interc nnected, as shown. Each phase shifter stage 40a″, 40b″ and 40c″ is similar to the digitally controlled phase shifter stage 40a described in conjunction with Figs. 6–8. Phase shifter stag 40a″ is here used, howev r, to provide a variable continuous phase shift between 0° and 90°. Phase
shifting stage 40b′ is used to produce a phase shift of φ = 0° or a phas shift of φ = 90°, and

phase shifter stage 40c'' is used to produce a phase shift of $\phi = 0°$ or $\phi = 180°$. The cascade interconnection of phase shifter stages 40a'', 40b'' and 40c'' provides the phase shifter 40'' which is capable of varying the phase of an input signal continuously over the range of 0° to 360°.

5   Referring also to Fig. 16–Fig. 17, an exemplary one of the stages 40a''–40c'' here 40a'' is formed on the substrate 41 having a ground plane 43. The phase shifter stage 40a'' is coupled to transmission line 32b of the transceiver 12i (Fig. 2). The phase shifter stage 40a'' includes a transmission line 512 coupled between the input matching network 513 as explained in conjunction with Fig. 5 and the transmission line 32b of transceiver 12i (Fig. 2). The matching
10   network 513 is coupled to input gate electrodes 532a, 532b of a pair of FET's 530a–530b, as shown. FET's 530a–530b further include control gate electrodes 534a–534b, source electrodes 538a–538b, and drain electrodes 536a–536b. FET's 530a–530b are fabricated, such that gains and phases provided to an input signal fed to the input gate electrodes 532a, 532b are substantially equal at the drain electrodes 536a, 536b, as explained in conjunction with Fig.6.
15   FET's 530a–530b are here connected in a common (grounded) source configuration, as shown. The control gate electrodes 534a–534b are fed voltage level control signal on control lines $29i_{3a}$, $29i_{3b}$. The radar system (Fig. 2) provides the control signals on lines $29i_{3a}$, $29i_{3b}$ (not shown in Fig. 2). The levels of such signals on the control lines $29i_{3a}$, $29i_{3b}$ are used to control the operating point of each FET and hence the amplitude of signals coupled to the drain
20   electrodes 536a, 536b. The drain electrodes 536a, 536b are electrically connected to capacitor 544 and impedance matching networks 545a, 545b as described in conjunction with Figs. 6–8. In the preferred embodiment of the invention, the impedance matching networks 545a, 545b are electrically connected to a conventional four port or quadrature coupler 1560. Such a coupler is described in an article entitled "GaAs Monolithic Lange and Wilkinson Couplers" by
25   Raymond C. Waterman, Jr, et al, IEEE Transactions on Electron Devices, Vol. ED–28, No. 2, February 1981. A quadrature coupler is here used to couple input signals on each input of the coupler, in quadrature, to the output. In other words, the phase of the input signal from drain electrode 536b as coupled to the output 1570 of the coupler will lag the phase of the input signal from drain electrode 536a as coupled to the output 1570 of the coupler by 90'.

30   Thus, unlike prior embodiments of the invention where signals fed to the control gate electrodes 534a–534b are complementary pairs of control signals, such signals provided to place an FET in an off-state or an on-state, the signals fed on lines $29i_{3a}$, $29i_{3b}$ to the control gate electrodes 534a, 534b, here are selectable voltage levels between pinchoff and zero volts "on" levels of such FET.

35   An output voltage signal V_o, when measured at the drain electrode, of an input signal V_i fed to the input gate electrode is given as: $V_i = A_oe^{j\omega t}$, is $V_0 = BA_oe^{j(\omega t + \psi)}$, for embodiments disclosed in conjunction with Figs. 5–14 where B is the gain and ψ is the phase provided to the input signal by the FET. However, if the control signals on lines $29i_{3a}$, $29i_{3a}$ fed to the control gates 534a–534b provide voltage level signals which change the operating point of the FET between
40   the off state and the on state, the FET's 530a, 530b no longer function as switches, and, instead the FETs 530a, 530b function as variable gain amplifiers. When the output voltage $V_0^{(A)}$ of the FET 530a is a function of the control gate voltage $V_{(g)}$ fed to control gate 534a, the portion of the output voltage V_{ot} at the output of the coupler 1560 from the voltage $V_0^{(A)}$ is given as: $V_o = B_AA_oe^{j(\omega t + \psi + \Delta\phi n)}$, where B_A is the gain of FET 530a as a function of the control gate
45   voltage, $\Delta\phi_n$ is the phase shift corresponding to the pathlength between the drain electrode of the nth FET and the output of the coupler 1560. The output voltage of FET 530a and FET 530b may be represented as:

$$V_o^{(A)}; \quad V_o^{(B)} \quad \text{where}$$

50   $$V_o^{(A)} = B_AA_oe^{j(\omega t + \psi)}; \quad V_o^{(B)} = B_BA_oe^{j(\omega t + \psi)}$$

Since the quadrature coupler 1560 combines the two input signals $V_o^{(A)}$ and $V_o^{(B)}$ in quadrature, the output voltage at the coupler 1560 may be represented as:

55   $$V_{oT} = V_o^{(A)} - jV_o^{(B)} \text{ or}$$
$$V_{oT} = B_AA_oe^{j(\omega t + \psi + \Delta\phi_A)} + B_BA_oe^{j(\omega t + \psi + \Delta\phi_n)} \text{ or}$$
$$V_{oT} = A_oe^{j(\omega t + \psi + \Delta\phi_A)}[B_A + B_Be^{-j\pi/2}]$$

which may be simplified to:

60   $$V_{oT} = A_o'B'e^{j\psi}$$

where $B' = (B_A^2 + B_B^2)^{\frac{1}{2}}$ and $\tan\theta = B_B/B_A$.
Thus, the phase of an input signal V_i (Fig. 15) is shifted in accordance with the ratio of th
65   amplitudes $V_o^{(A)}$, $V_o^{(B)}$ of such input signal as coupled to each drain electrode 536a, 536b   65

coupled in quadrature to provide the signal V_{o1} (Fig. 15) at th output of the quadrature coupler 1560.

Thus by sel cting the relative valu s of B_1 and B_2 any phas b tween 0 and $\pi/2$ may be realized. Since only the ratio of B_1 and B_2 determines the phase, it is possible to keep B' and
5 hence the overall gain of the stage 40a'' substantially constant. This is accomplished by   5
separately adjusting the values of B_1 and B_2. This provides an additional flexibility of amplitude control along with phase adjustment.

As an example, for a minimum phase shift increment of $\pi/16$, the values of B_1 and B_2 which will yield all eight phase shift increments between 0 and $\pi/2$ with substantially constant
10 amplitude B' are given in the Table below.   10

TABLE

Phase Shift	b_1	b_2
0	1.000	0
$\pi/16$	0.981	0.195
$\pi/8$	0.924	0.383
$3\pi/16$	0.832	0.556
$\pi/4$	0.707	0.707
$5\pi/16$	0.556	0.832
$3\pi/8$	0.383	0.924
$7\pi/16$	0.195	0.981
$\pi/2$	0	1.000

where:

$b_1 B' = B_1$

$b_2 B' = B_2$

The minimal phase shift increment provided by the variable phase shift stage 40a'' is limited
30 only by the degree of control of the voltage applied to the control gate electrodes 534a–534b   30
of FET 530a–530b of phase shifter stage 40a''.

Phase shift stage 40a'' is cascade interconnected to phase shift stage 40b'', as shown. The phase shift stage 40b'' is identical to phase shift stage 40a''. The only difference between the stages 40a'' and 40b'', is the technique for producing the phase shift. A phase shift of 0° or
35 90° provided by phase shifter stage 40b'' is determined by controlling which FET 530a–530b   35
is biased in the on state, as previously described in conjunction with Figs. 6–8.

Phase shift 40c'' stage is similar to phase shift stage 40a'' except for the inclusion of an _ additional 90° of path-length difference such as transmission line section 554b (Fig. 9b) coupled between the impedance matching network 545a and the coupler 1560.
40   Referring now to Figs. 18–19, bidirectional switch 18a having a first branch port 19a   40
coupled to transmission line 32a (Fig. 2), a second branch port 21a, coupled to transmission line 32h (Fig. 2), and a common port 20a coupled to transmission line 33i, (Fig. 2), is shown. The bidirectional switch 18a is formed on the substrate 41, having the ground plane 43 formed on the bottom surface of substrate 41, as shown. FETs 501–50b are formed on a portion of the
45 substrate 41. In the preferred embodiment, FET's 50a, 50b include a plurality of FET cells,   45
each cell having a reactive component (C'') coupled between the drain and source electrode of each cell as shown in Fig. 20. A network, here the FET 50a is formed interconnecting each one of such drain electrodes of each FET cell. Such network is formed having a characteristic impedance equal to the characteristic impedance of the transmission line sections 58a, 58b,
50 here 50 ohms. The network is formed as follows: a length (d) of a microstrip conductor 59   50
having a distributed inductance per unit length (L_L) and a distributed capacitance per unit length (C_L) is chosen such that when coupled between the cells of each FET it will provide such network with the predetermined characteristic impedance given as: $Z_o = (L_L(C_L + 2(C''/d)))^{1/2}$.
The bidirectional switch further includes a pair of transmission lines 58a–58b, each having a
55 electrical length substantially equal to one quarter of a wavelength ($\lambda_c/4$) where λ_c is the   55
wavelength of the nominal op rating frequency for the circuit. The first drain electrode 54a of FET 50a is coupled between the first branch p rt 19a and to one end f transmission line 58a. The transmission line 58a is coupled between the branch port 19a and the common port 20a. A drain electrode 54b of a second FET 50b is coupled to the second branch port 21a, and one
60 end of the transmission line 58b. The other end of transmission line 58b is coupled to the   60
common port 20a. The sources 56a–56b of FET 50a–50b are electrically connected to ground.
Th gate lectrodes 52a–52b of FET's 50a–50b are el ctrically connect d to control lines 29_{ii},
$\overline{29_{ii}}$, and are fed complementary signals on such lines.

The T/R switch 18a is used to couple a signal, n transmission line 33i of the transceiver 12i
65 (Fig. 2) fed to the common port 20a to on of the branch ports 19a or 21a in acc rdance with a   65

pair of complementary c ntrol signals on lines 29i,, $\overline{29i}$,, fed to gat electrodes 52a, 52b. The T/R switch 18a couples an input signal from common port 20a to branch port 1 9a, as follows: the control signal on line 29i,, is fed to the gate lectrode 52a of FET 50a, placing FET 50a in a nonconducting state; correspondingly, the control signal fed on line $\overline{29i}$, is applied to the gate
5 electrode 52b of FET 50b placing FET 50b in a conducting state; by placing FET 50b in a   5
conducting state, a short circuit Ⓢ (low impedance path to ground) is produced at the end 58b' of transmission line 58b coupled to the drain electrode 54b; one quarter of a wavelength from this point (at the second end of transmission line 58b) the short circuit at the first end appears as an open circuit Ⓞ (high impedance) to a microwave frequency signal having a wavelength
10 substantially similar to the wavelength of the corresponding centerband frequency of operation   10
for the bidirectional switch 18a. The transmission line 58a and the open circuit resulting from FET 50a being in a nonconducting state, appears as a 50 ohm transmission line at the common port side 58a' of the transmission line 58a. Thus, a signal on common port 20a is coupled to the branch port 19a. In a similar manner, by changing the state of the complementary pair of
15 control signals on lines 29i,, $\overline{29i}$,, a microwave frequency signal on common port 20a may be   15
coupled to the branch port 21a.
   Having described preferred embodiments of the invention, it will now become readily apparent to those of skill in the art that other embodiments incorporating the invention may be realized. It is felt, therefore, that this invention should not be limited to the disclosed
20 embodiments but rather should be limited only to the scope of the appended claims.   20
   Matter described hereinbefore is described and claimed in co-pending patent application No. 8305509 from which the present application is divided.

   CLAIMS
25   1.   A transceiver element for coupling electromagnetic energy between a pair of terminals   25
comprising:
      a phase shifter;
      a transmitter amplifier;
      a receiver amplifier; and
30   a switching means for steering electromagnetic energy from one of the terminals through the   30
phase shifter, through the transmitter amplifier, and to the second terminal during a transmit mode; and for steering electromagnetic energy from the second terminal through the receiver amplifier through the phase shifter, and to the first terminal during a receive mode; such that the electromagnetic energy passes through the phase shifter in the same direction during the
35 transmit and receive modes.   35
   2.   A transceiver element according to claim 1, wherein the phase shifter provides gain to transmitted and received electromagnetic energy as such electromagnetic energy propagates through the phase shifter.
   3.   A transceiver element according to claim 1, wherein the switching means comprises: a
40 plurality of switches, each one of such switches having a common port and a pair of branch   40
ports; the common port of each one of a first pair of such switches is coupled to a corresponding one of such pair of terminals of the transceiver element; the common port of each one of a second different pair of such switches is coupled to a corresponding one of the pair of terminals of the phase shifter; the branch ports of a first one of such first pair of switches are
45 coupled to corresponding first branch ports of each one of the second pair of switches; and the   45
branch ports of a second one of such first pair of switches are coupled by the said amplifiers to second branch ports of each one of such second pair of switches.
   4.   A transceiver element according to claim 1, wherein the switch means comprises: a first pair of transmission lines coupled together at a first common junction and to a first one of the
50 pair of terminals of the radio frequency circuit; a second pair of transmission lines coupled   50
together at a second common junction and to a first one of the pair of terminals of the phase shifter, having a first end coupled to a first end of the first pair of transmission lines, and having a second end coupled to the receiver amplifier; a third pair of transmission lines coupled together at a third common junction and to a second one of the pair of terminals of the phase
55 shifter, having a first end coupled to a second end of the first pair of transmission lines, and   55
having a second end coupled to the transmitter amplifier; a first pair of transistors, each transistor having output and control l ctrodes, with the output lectrode of each one of such transistors being coupled to a corresponding end of th second pair of transmission lines; and a second pair of transistors, each transistor having output and control electrodes, with th output
60 electrode of each one of such transistors being coupled to a corresponding end of the third pair   60
of transmission lines.
   5.   A transceiver element according to claim 4, wherein there is provided a switch having a common port and a pair of branch p rts with the common port coupled to a s cond one of a pair of t rminals of the transceiver, and each one of th branch ports of the said switch coupled
65 to a corresponding one of such amplifiers.   65

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6. A transc iver element according to claim 5, wherein a first control signal is fed to first transistors of each pair of transistors and a second different control signal is fed to second transistors of each pair of transistors to steer electromagnetic energy through the phase shifter and through the receiver amplifier in response to a first state of th control signals and to steer
5 electromagnetic energy through the phase shifter and through the transmitter amplifier in response to a second, different state of the control signals.

7. A transceiver element according to claim 5, wherein each one of such transmission lines has an electrical length equal to an odd multiple of a quarter of a wavelength of a corresponding operating frequency.

10 8. A transceiver element according to claim 1, wherein the phase shifter further comprises:
(i) a first independently controllable phase shifter channel having a first pair of terminals;
(ii) a second independently controlled phase shift channel having a second pair of terminals;
wherein the switching means further comprises:
(i) a pair of switches having a common port and a pair of branch ports;
15 wherein the common port of each one of the switches is coupled to a corresponding one of the pair of terminals of the transceiver elements, a first branch port of a first one of the switches is coupled to an input one of the pair of terminals of the first phase shift channel, a second branch port of the first switch is coupled to an output one of the pair of terminals of the second channel, and each one of the branch ports of the second switch is coupled through one of such
20 amplifiers to a corresponding remaining one of the pair of terminals of the first and second channels.

9. A microwave transceiver element susbtantially as described hereinbefore with reference to Figs. 2 or 3 of the accompanying drawings.

10. A microwave transceiver element substantially as described hereinbefore with reference
25 to Fig. 4 of the accompanying drawings.

11. A microwave transceiver element according to claim 9 and susbtantially as described hereinbefore with reference to Figs. 5, 6, 7 and 8 of the accompanying drawings.

12. A microwave transceiver element according to claim 10 and substantially as described hereinbefore with reference to Figs. 10 and 11 of the accompanying drawings.

30 13. A microwave transceiver element according to claim 12 and substantially as described hereinbefore with reference to Fig. 12 of the accompanying drawings.

14. A microwave transceiver element according to claim 9 and substantially as described hereinbefore with reference to Fig. 13 of the accompanying drawings.

15. A microwave transceiver element according to claim 9 or 10 and substantially as
35 described hereinbefore with reference to Fig. 14 of the accompanying drawings.

16. A microwave transceiver element according to claim 9 and substantially as described hereinbefore with reference to Fig. 15 of the accompanying drawings.

17. A microwave transceiver element according to claim 16 and substantially as described hereinbefore with reference to Figs. 16 and 17 of the accompanying drawings.

40 18. A microwave transceiver element according to any preceding claim and substantially as described hereinbefore with reference to Figs. 18 to 20 of the accompanying drawings.

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